

**$\mu$ PD78001B(A), 78002B(A)****8-BIT SINGLE-CHIP MICROCOMPUTER****DESCRIPTION**

The  $\mu$ PD78001B(A)/78002B(A) are products in the  $\mu$ PD78002 subseries within the 78K/0 series.

The  $\mu$ PD78001B(A)/78002B(A) have various peripheral hardware such as timer, serial interface and interrupt function.

A one-time PROM or EPROM product, the  $\mu$ PD78P014, capable of operating in the same power supply voltage range as that of the mask ROM product and other development tools is provided.

Functions are described in detail in the following User's Manual, which should be read when carrying out design work.

**$\mu$ PD78002, 78002Y Series User's Manual: IEU-1334**

**FEATURES**

- The  $\mu$ PD78001B, in comparison with the 78002B, is a higher reliability device, as a result of a more comprehensive quality assurance program (Refer to Quality Grade on NEC Semiconductor Devices (IEI-1209))
- Large on-chip ROM & RAM

Item Product Name	Program Memory (ROM)	Data Memory (Internal High-Speed RAM)	Package
$\mu$ PD78001B(A)	8K bytes	256 bytes	• 64-pin plastic shrink DIP (750 mil)
$\mu$ PD78002B(A)	16K byte	384 bytes	• 64-pin plastic QFP ( $\square$ 14 mm)

- External memory expansion space: 64K bytes
- Instruction execution time can be varied from high-speed (0.4  $\mu$ s) to ultra-low-speed (122  $\mu$ s)
- I/O ports: 53 (N-ch open-drain : 4)
- Serial interface : 1 channel
- Timer: 4 channels
- Operating voltage range : 2.7 to 6.0 V

**APPLICATION**

Transmission equipment control device, gas detector circuit breaker, safety devices, etc.

The information in this document is subject to change without notice.

# ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD78001BCW (A)-xxx	64-pin plastic shrink DIP (750 mil)	Special
μPD78001BGC (A)-xxx-AB8	64-pin plastic QFP (□14 mm)	Special
μPD78002BCW (A)-xxx	64-pin plastic shrink DIP (750 mil)	Special
μPD78002BGC (A)-xxx-AB8	64-pin plastic QFP (□14 mm)	Special

**Remark** xxx indicates ROM code No.

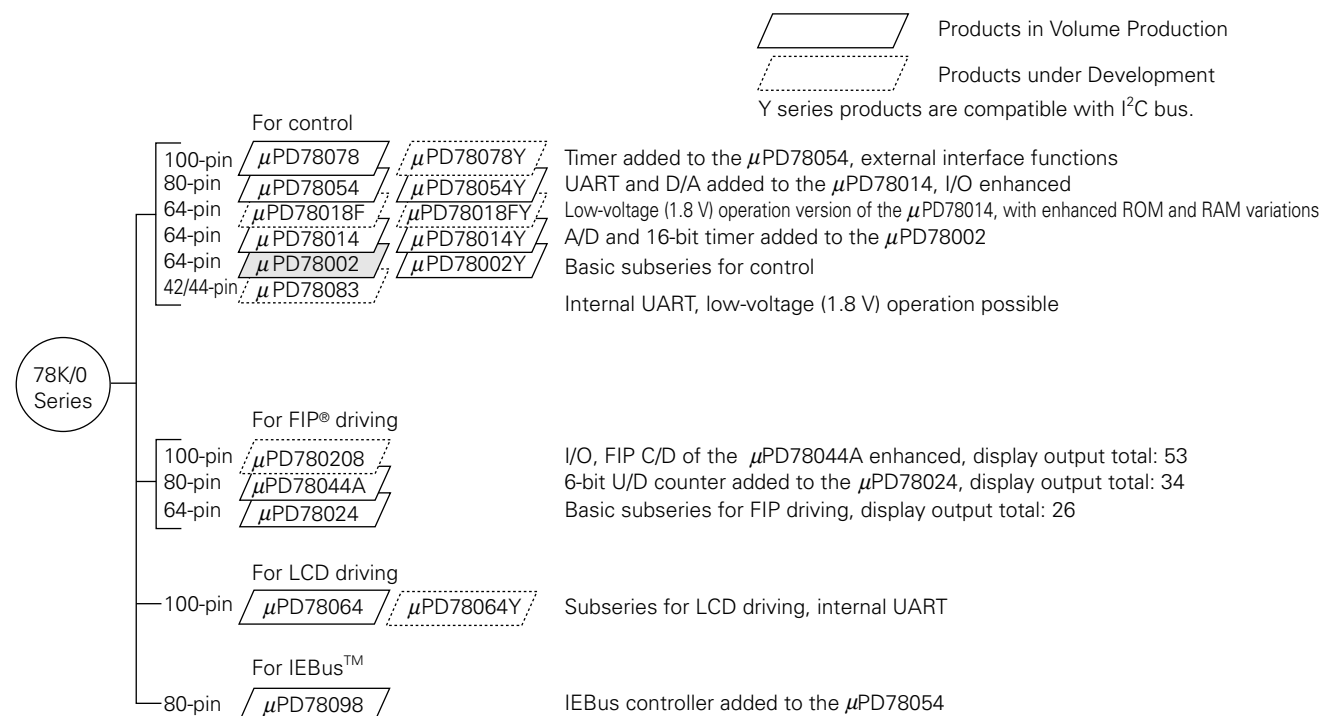
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

## Difference between the μPD78001B(A), 78002B(A) and the μPD78001B, 78002B.

Product Name	μPD78001B(A), 78002B(A)	μPD78001B, 78002B
Item		
Quality Grade	Special	Standard

## 78K/0 SERIES PRODUCT DEVELOPMENT

These products are a further development in the 78K/0 Series. The designations appearing inside the boxes are subseries names.



The major functional differences among the subseries are shown below.

Function Name		Timer				A/D	D/A	Serial Interface	I/O	V <sub>DD</sub> MIN. Value	External Expansion
		8-bit	16-bit	Watch	Watchdog						
For Control	μPD78078	4ch	1ch	1ch	1ch	8-bit × 8ch	8-bit × 2ch	3ch (UART: 1ch)	88	1.8 V	C
	μPD78054	2ch							69	2.0 V	
	μPD78018F						—	2ch	53	1.8 V	
	μPD78014									2.7 V	
	μPD78002		—			—		1ch			
	μPD78083			—		8-bit × 8ch		1ch (UART: 1ch)	33	1.8 V	—
For FIP® driving	μPD780208	2ch	1ch	1ch	1ch	8-bit × 8ch	—	2ch	74	2.7 V	—
	μPD78044A								68		
	μPD78024								54		
For LCD driving	μPD78064	2ch	1ch	1ch	1ch	8-bit × 8ch	—	2ch (UART: 1ch)	57	2.0 V	—
For IEBus™	μPD78098	2ch	1ch	1ch	1ch	8-bit × 8ch	8-bit × 2ch	3ch (UART: 1ch)	69	2.7 V	C

## OVERVIEW OF FUNCTION

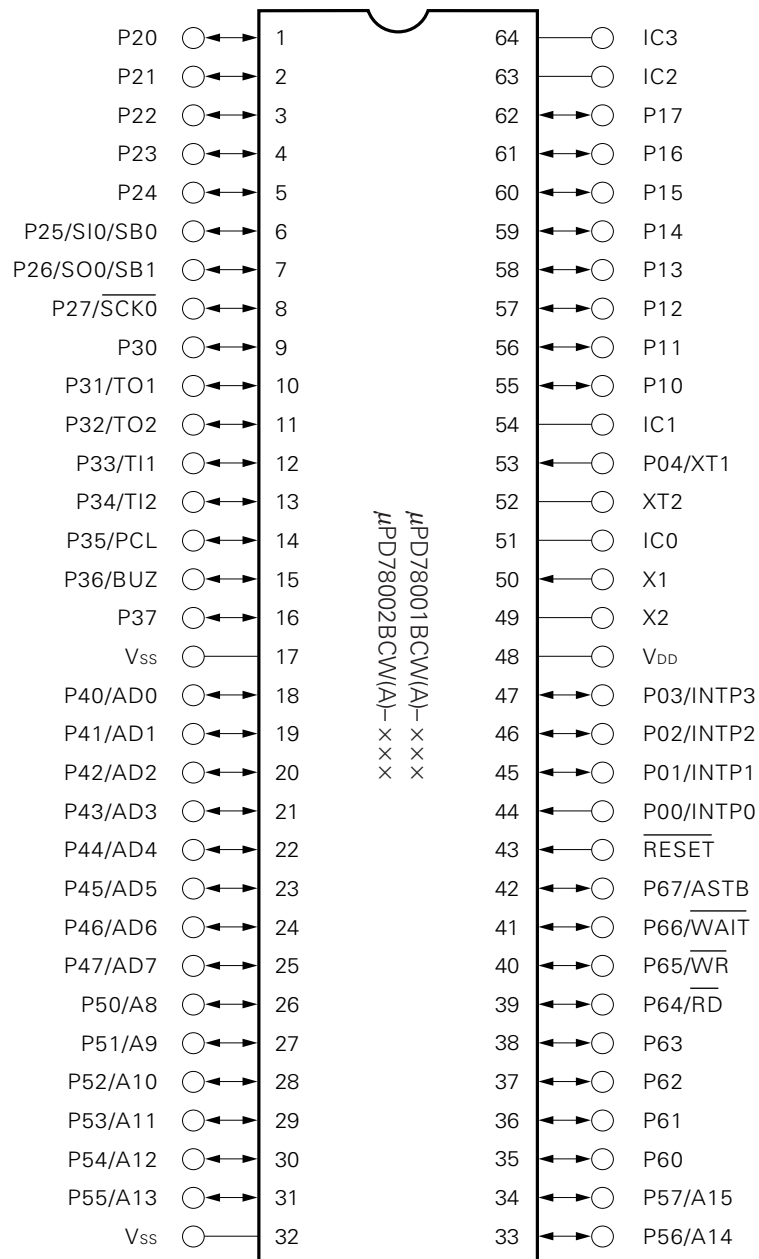
Product Name Item		$\mu$ PD78001B(A)	$\mu$ PD78002B(A)
Internal memory	ROM	8K bytes	16K bytes
	Internal high-speed RAM	256 bytes	384 bytes
Memory space		64K bytes	
General registers		8 bits $\times$ 32 registers (8 bits $\times$ 8 registers $\times$ 4 banks)	
Instruction cycle		On-chip instruction execution time cycle modification function	
	When main system clock selected	0.4 $\mu$ s/0.8 $\mu$ s/1.6 $\mu$ s/3.2 $\mu$ s/6.4 $\mu$ s (at 10.0 MHz operation)	
	When subsystem clock selected	122 $\mu$ s (at 32.768 kHz operation)	
Instruction set		<ul style="list-style-type: none"> <li>• 16-bit operation</li> <li>• Bit manipulation (set, reset, test, boolean operation)</li> <li>• BCD correction, etc.</li> </ul>	
I/O ports		Total : 53 <ul style="list-style-type: none"> <li>• CMOS input : 2</li> <li>• CMOS I/O : 47</li> <li>• N-channel open-drain I/O (15 V withstand voltage) : 4</li> </ul>	
Serial interface		<ul style="list-style-type: none"> <li>• 3-wire/SBI/2-wire mode selectable</li> </ul>	
Timer		<ul style="list-style-type: none"> <li>• 8-bit timer/event counter : 2 channels</li> <li>• Watch timer : 1 channel</li> <li>• Watchdog timer : 1 channel</li> </ul>	
Timer output		2	
Clock output		39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz (at main system clock 10.0 MHz operation), 32.768 kHz (at subsystem clock 32.768 kHz operation)	
Buzzer output		2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock 10.0 MHz operation)	
Vectored interrupts	Maskable interrupts	Internal : 5 External: 4	
	Non-maskable interrupt	Internal : 1	
	Software interrupt	Internal : 1	
Test input		Internal : 1 External : 1	
Operating voltage range		V <sub>DD</sub> = 2.7 to 6.0 V	
Operating ambient temperature range		-40 to +85°C	
Package		<ul style="list-style-type: none"> <li>• 64-pin plastic shrink DIP (750 mil)</li> <li>• 64-pin plastic QFP (<math>\square</math>14 mm)</li> </ul>	

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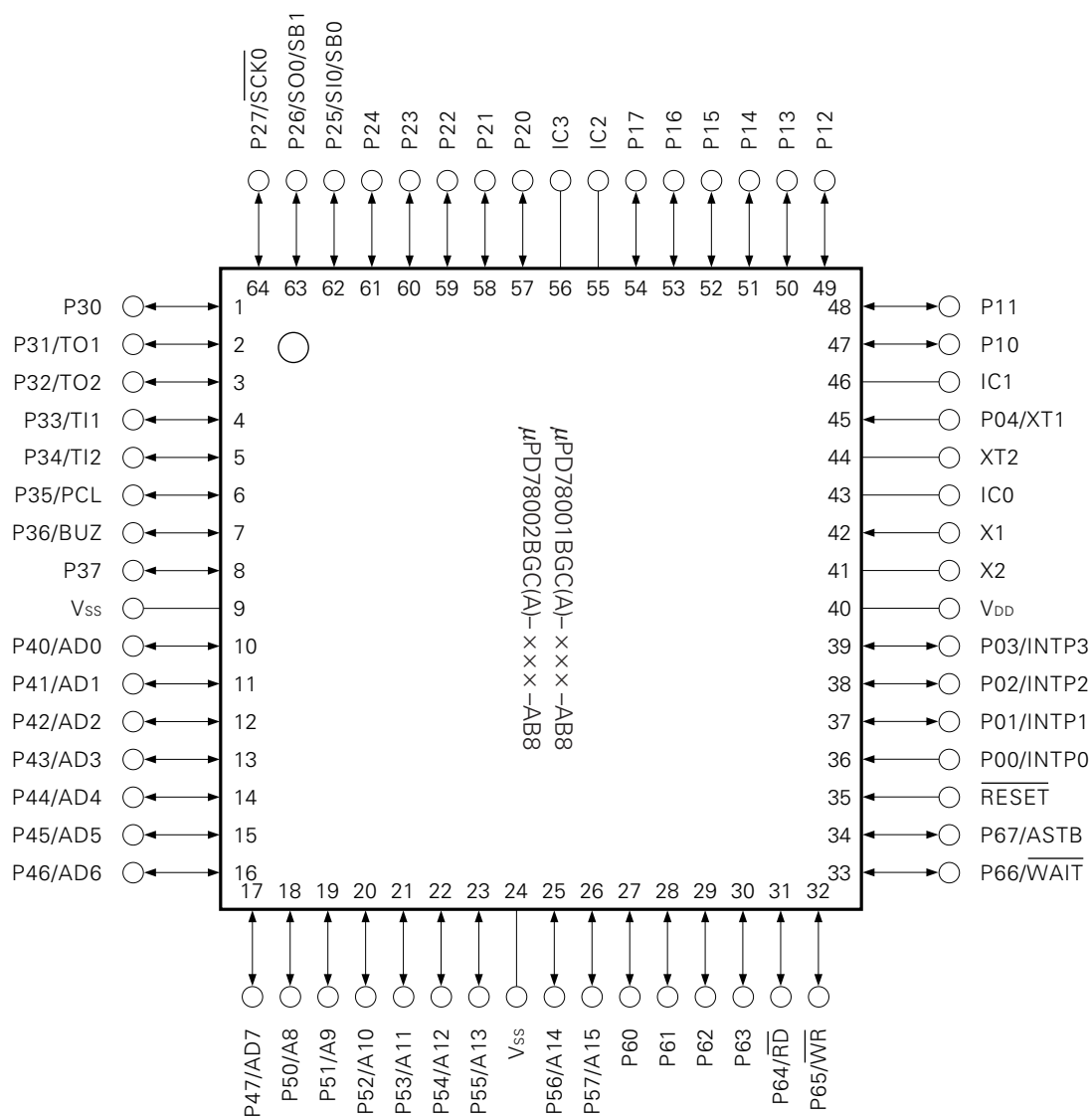
## 1. PIN CONFIGURATION (TOP VIEW)

## 64-Pin Plastic Shrink DIP (750 mil)



**Remark** Always connect the IC0, IC1 and IC3 (Internally Connected) pins to V<sub>SS</sub> directly.  
Always connect the IC2 pin to V<sub>DD</sub> directly.

64-Pin Plastic QFP (□14 mm)

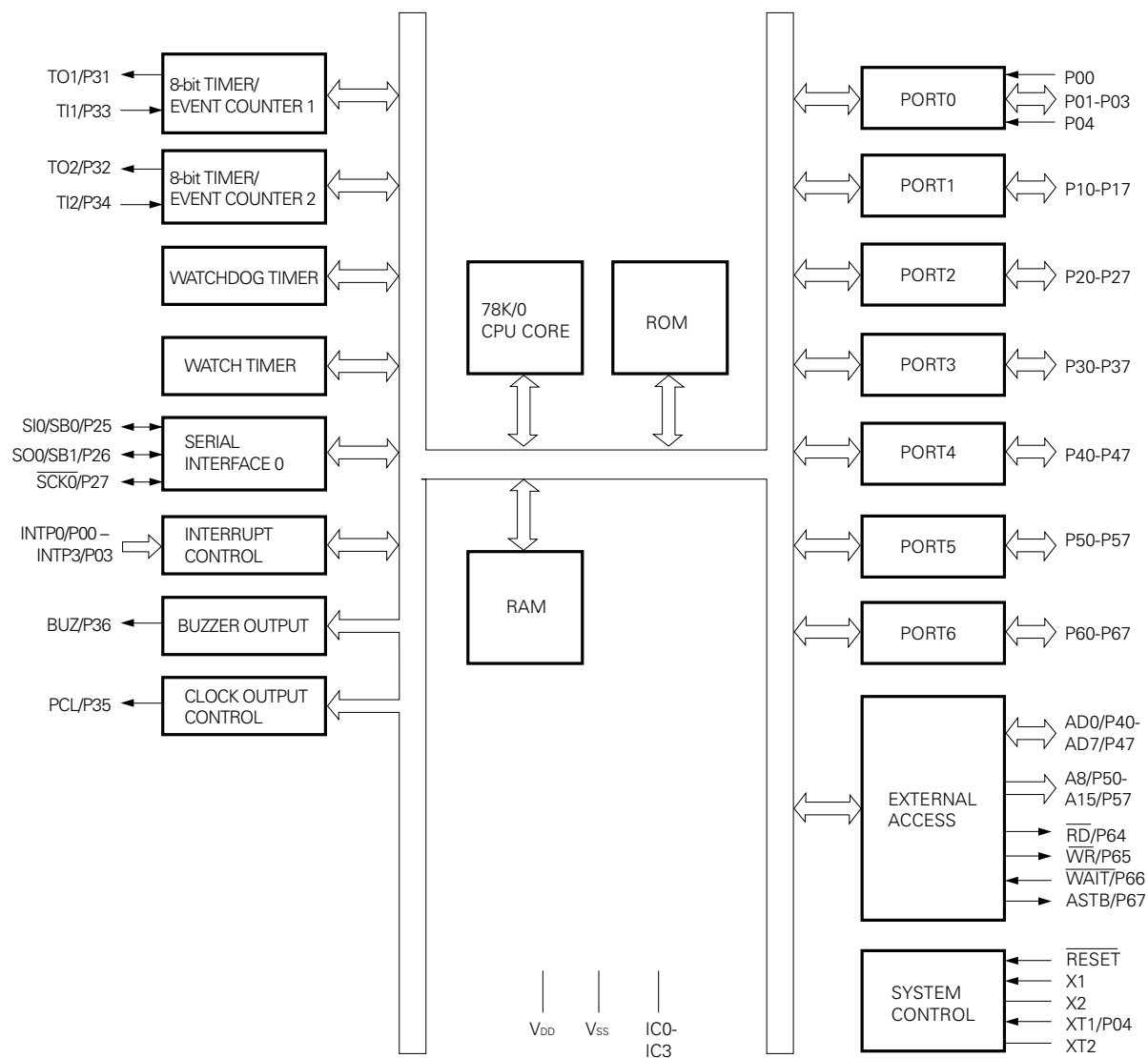


**Remark** Always connect the IC0, IC1 and IC3 (Internally Connected) pins to Vss directly.  
Always connect the IC2 pin to VDD directly.

P00 to P04	: Port 0	PCL	: Programmable Clock
P10 to P17	: Port 1	BUZ	: Buzzer Clock
P20 to P27	: Port 2	AD0 to AD7	: Address/Data Bus
P30 to P37	: Port 3	A8 to A15	: Address Bus
P40 to P47	: Port 4	$\overline{\text{RD}}$	: Read Strobe
P50 to P57	: Port 5	$\overline{\text{WR}}$	: Write Strobe
P60 to P67	: Port 6	WAIT	: Wait
INTP0 to INTP3	: Interrupt From Peripherals	ASTB	: Address Strobe
TI1, TI2	: Timer Input	X1, X2	: Crystal (Main System Clock)
TO1, TO2	: Timer Output	XT1, XT2	: Crystal (Subsystem Clock)
SB0, SB1	: Serial Bus	$\overline{\text{RESET}}$	: Reset
SI0	: Serial Input	V <sub>DD</sub>	: Power Supply
SO0	: Serial Output	V <sub>SS</sub>	: Ground
SCK0	: Serial Clock	IC0 to IC3	: Internally Connected



## 2. BLOCK DIAGRAM



**Remark** Internal ROM & RAM capacity varies depending on the product.

### 3. PIN FUNCTIONS

#### 3.1 PORT PINS (1/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P00	Input	Port 0 5-bit I/O port	Input only	Input	INTP0
P01	Input/ output		Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.	Input	INTP1
P02					INTP2
P03					INTP3
P04*	Input		Input only	Input	XT1
P10 to P17	Input/ output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.			–
P20	Input/ output	Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.		Input	–
P21					–
P22					–
P23					–
P24					–
P25					SI0/SB0
P26					SO0/SB1
P27					SCK0
P30	Input/ output	Port 3 8-bit input/output port. Input/output can be specified in bit-wise. When used as an input port, pull-up resistor can be used by software.		Input	–
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					–
P40 to P47	Input/ output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit unit. When used as an input port, pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

\* When using the P04/XT1 pins as an input port, set 1 to bit 6 (FRC) of the processor control register. (Do not use the on-chip feedback register of the subsystem clock oscillator.)

## 3.1 PORT PINS (2/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P50 to P57	Input/output	Port 5 8-bit input/output port. LED can be driven directly. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.		Input	A8 to A15
P60	Input/output	Port 6 8-bit input/output port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.	Input	————
P61					
P62					
P63					
P64		When used as an input port, pull-up resistor can be used by software.	$\overline{\text{RD}}$		
P65			$\overline{\text{WR}}$		
P66			$\overline{\text{WAIT}}$		
P67			ASTB		

**Caution** When pull-up resistors are not used (specified by mask option), the low-level input leak current increases with  $-200\ \mu\text{A}$  (MAX.) under either of the following conditions.

- ① When the external device expansion function is used and a low-level is input to the pin.
- ② During the 3-clock period when a read instruction is executed on port 6 (P6) and the port mode register (PM6).

## 3.2 OTHER PINS

Pin Name	I/O	Function	After Reset	Dual-Function Pin
INTP0	Input	Effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00
INTP1				P01
INTP2		External interrupt input.		P02
INTP3		Falling edge detection external interrupt input.		P03
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SB0	Input /output	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
SCK0	Input /output	Serial interface serial clock input/output.	Input	P27
TI1	Input	External count clock input to 8-bit timer (TM1).	Input	P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO1	Output	8-bit timer (TM1) output.	Input	P31
TO2		8-bit timer (TM2) output.		P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
AD0 to AD7	Input /output	Low-order address/data bus at external memory expansion.	Input	P40 to P47
A8 to A15	Output	High-order address bus at external memory expansion.	Input	P50 to P57
$\overline{\text{RD}}$	Output	External memory read operation strobe signal output.	Input	P64
$\overline{\text{WR}}$		External memory write operation strobe signal output.		P65
$\overline{\text{WAIT}}$	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output which latches the address information output at port 4 and port 5 to access external memory.	Input	P67
$\overline{\text{RESET}}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P04
XT2	—		—	—
V <sub>DD</sub>	—	Positive power supply.	—	—
V <sub>SS</sub>	—	Ground potential.	—	—
IC0 to IC3	—	Internal connection. IC0/IC1/IC3 and IC2 should be connected directly to V <sub>SS</sub> V <sub>DD</sub> , respectively.	—	—

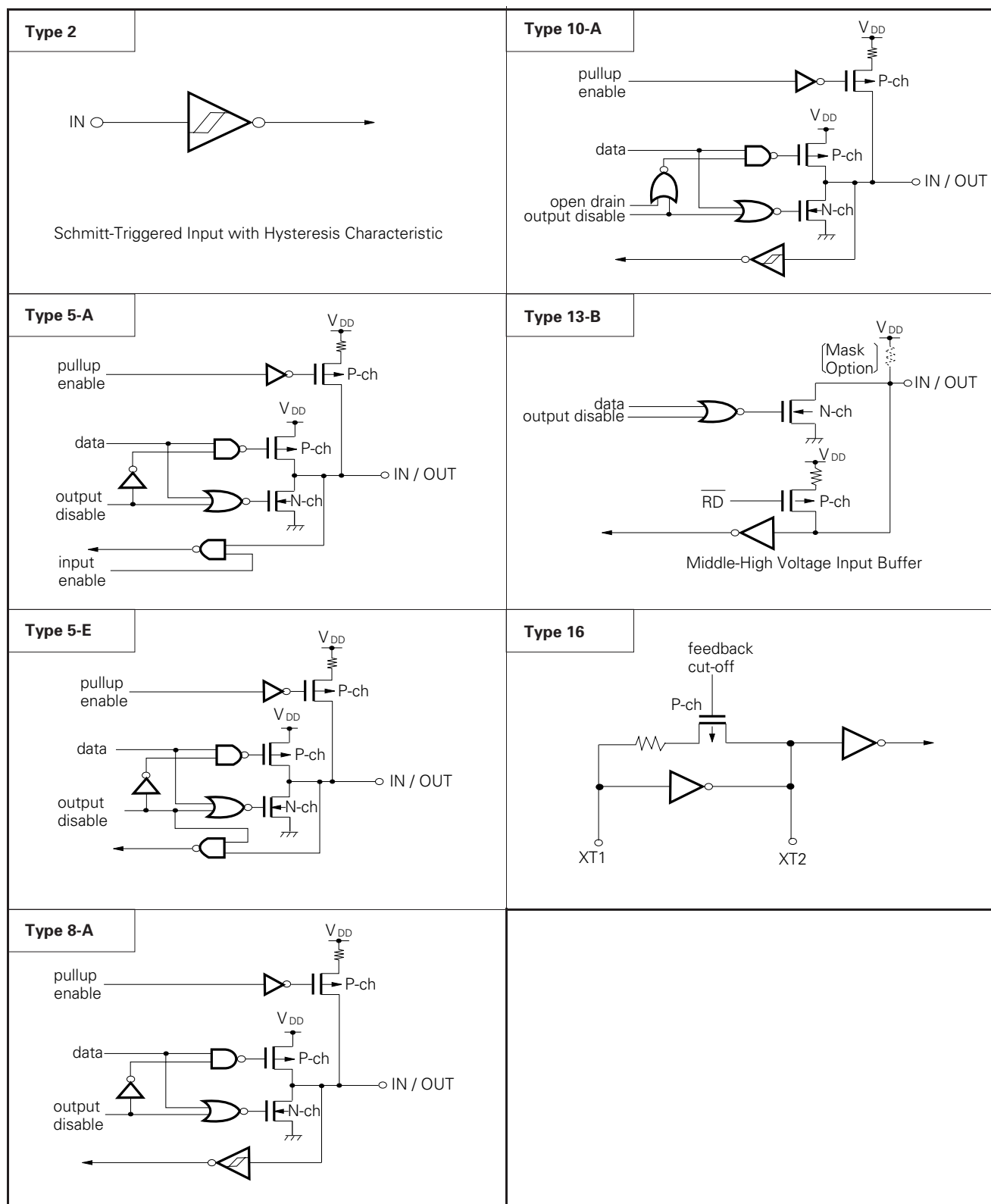
### 3.3 PIN I/O CIRCUIT AND RECOMMENDED CONNECTION OF UNUSED PINS

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.  
For the input/output circuit configuration of each type, see Fig. 3-1.

**Table 3-1 Input/Output Circuit Type of Each Pin**

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection when Not Used
P00/INTP0	2	Input	Connected to Vss .
P01/INTP1	8-A	Input/output	Connected to Vss through resistor independently.
P02/INTP2			
P03/INTP3			
P04/XT1	16	Input	Connected to VDD or Vss .
P10 to P17	5-A	Input/output	Connected to VDD or Vss through resistor independently.
P20 to P24			
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/SCK0			
P30	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-E		Connected to VDD through resistor independently.
P50/A8 to P57/A15	5-A		Connected to VDD or Vss through resistor independently.
P60 to P63	13-B		Connected to VDD through resistor independently.
P64/RD	5-A		Connected to VDD or Vss through resistor independently.
P65/WR			
P66/WAIT			
P67/ASTB			
RESET	2	Input	—
XT2	16	—	Leave open.
IC0, IC1, IC3	—		Connected to Vss directly.
IC2			Connected to VDD directly.

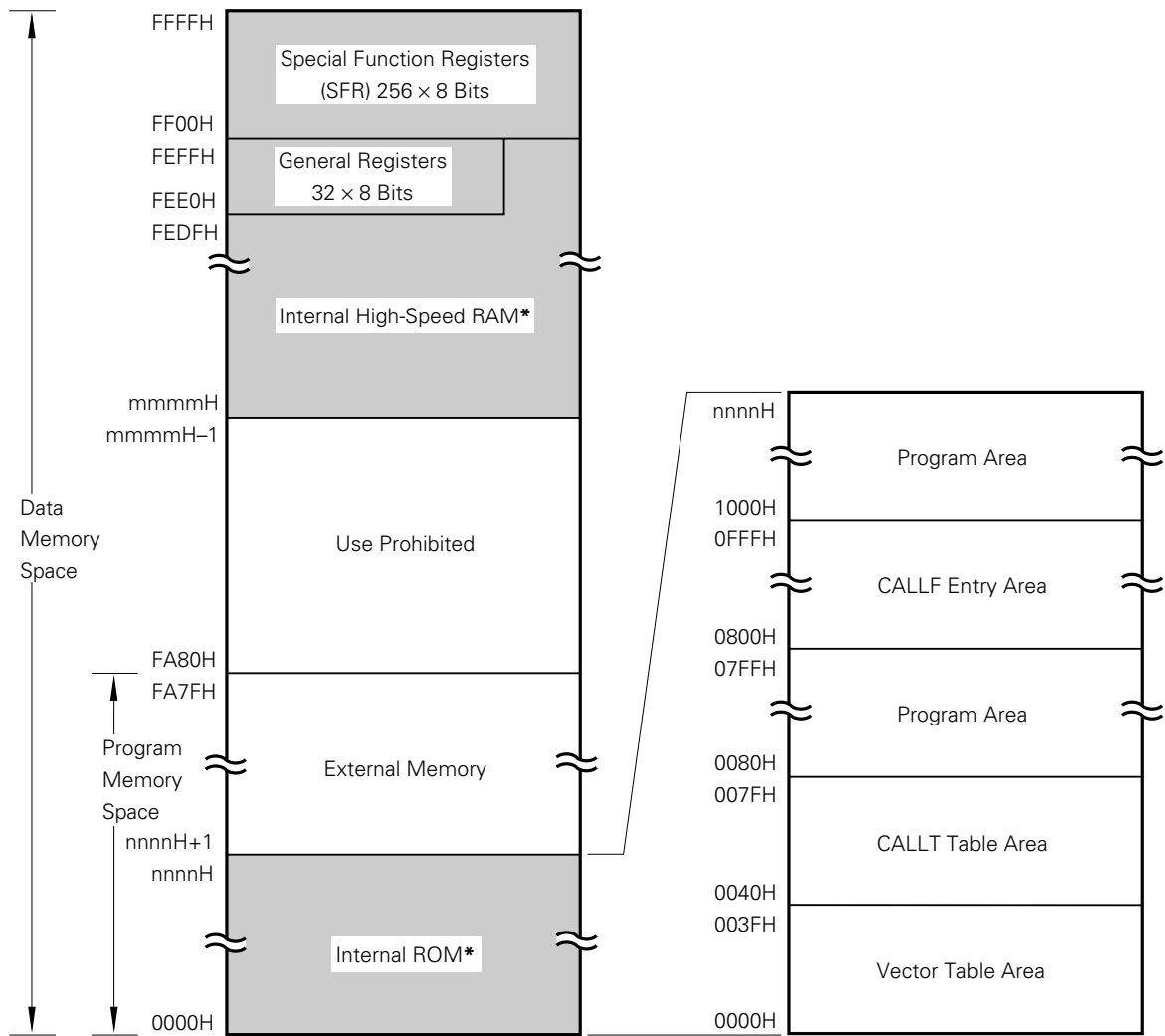
Fig. 3-1 Pin Input/Output Circuits



4. MEMORY SPACE

The memory map of μPD78001B(A)/78002B(A) is shown in Fig. 4-1.

Fig. 4-1 Memory Map



**Remark** Shaded area indicates internal memory.

\* Internal ROM and internal high-speed RAM capacities vary depending on the product (see the table below).

Product Name	Internal ROM End Address nnnnH	Internal High-Speed RAM Start Address mmmmH
μPD78001B(A)	1FFFH	FE00H
μPD78002B(A)	3FFFH	FD80H

## 5 PERIPHERAL HARDWARE FUNCTION FEATURES

### 5.1 PORTS

The I/O port has the following three types.

- CMOS input (P00, P04) : 2
  - CMOS input/output (P01 to P03,  
port 1 to port 5, P64 to P67) : 47
  - N-ch open-drain input/output  
(15V withstand voltage) (P60 to P63) : 4
- 
- Total : 53

**Table 5-1 Functions of Ports**

Port Name	Pin Name	Function
Port 0	P00, P04	Dedicated Input port
	P01 to P03	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.
Port 1	P10 to P17	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.
Port 2	P20 to P27	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.
Port 3	P30 to P37	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.
Port 4	P40 to P47	Input/output ports. Input/output can be specified in 8-bit units. When used as an input port, pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software. LED can be driven directly.
Port 6	P60 to P63	N-ch open-drain input/output port. Input/output can be specified bit-wise. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.
	P64 to P67	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.

**Caution** When pull-up resistors are not used (specified by mask option), low-level input leak current increases with  $-200\ \mu\text{A}$  (MAX.) under either of the following conditions.

- ① When the external device expansion function is used and a low-level is input to the pin.
- ② During the 3-clock period when a read instruction is executed on port 6 (P6) and the port mode register (PM6).

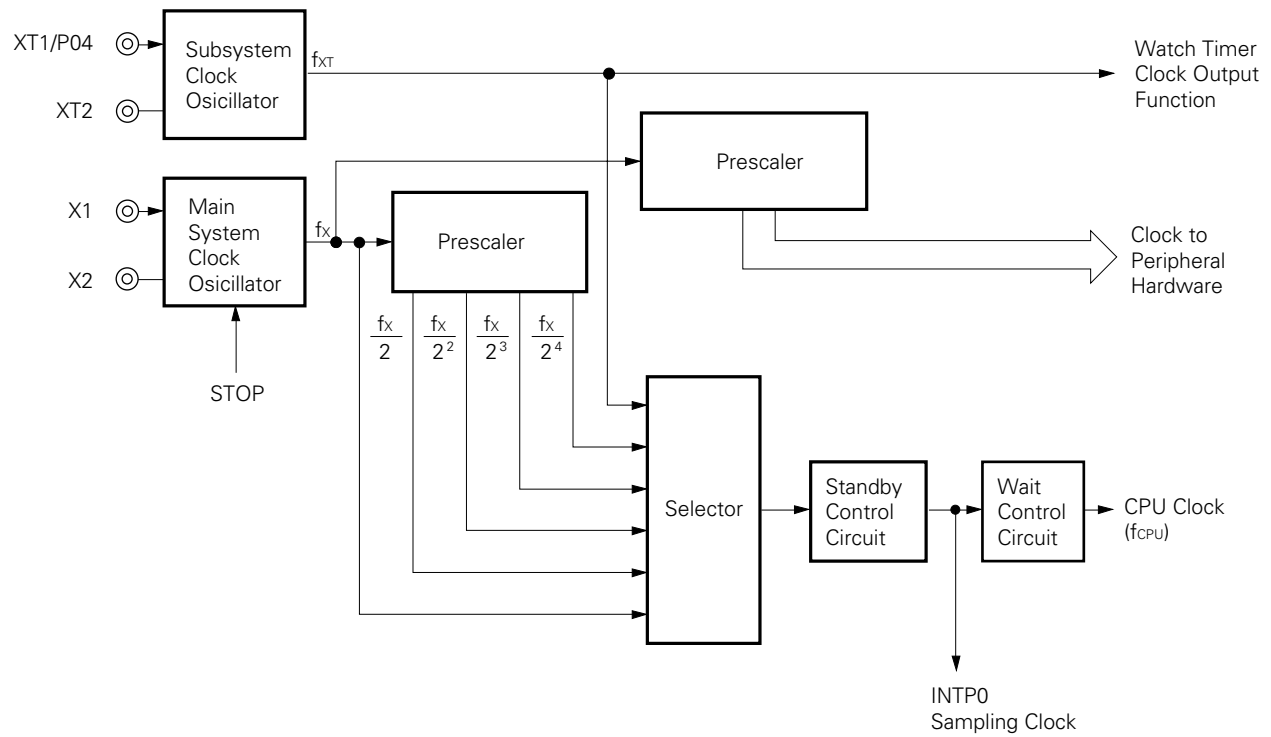


## 5.2 CLOCK GENERATOR

There are two types of clock generator: main system clock and subsystem clock.  
The instruction execution time can be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (mainsystem clock: at 10.0 MHz operation)
- 122 μs (subsystem clock: at 32.768 KHz operation)

Fig. 5-1 Clock Generator Block Diagram



### 5.3 TIMER/EVENT COUNTER

The following four channels are incorporated in the timer/event counter.

- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

**Table 5-2 Types and Features of Timer/Event Counter**

		8-bit Timer/Event Counter	Watch Timer	Watchdog Timer
Type	Interval timer	2 channels	1 channel	1 channel
	External event counter	2 channels	–	–
Functions	Timer output	2 outputs	–	–
	Square wave output	2 outputs	–	–
	Interrupt request	2	2	1

**Fig. 5-2 8-Bit Timer/Event Counter Block Diagram**

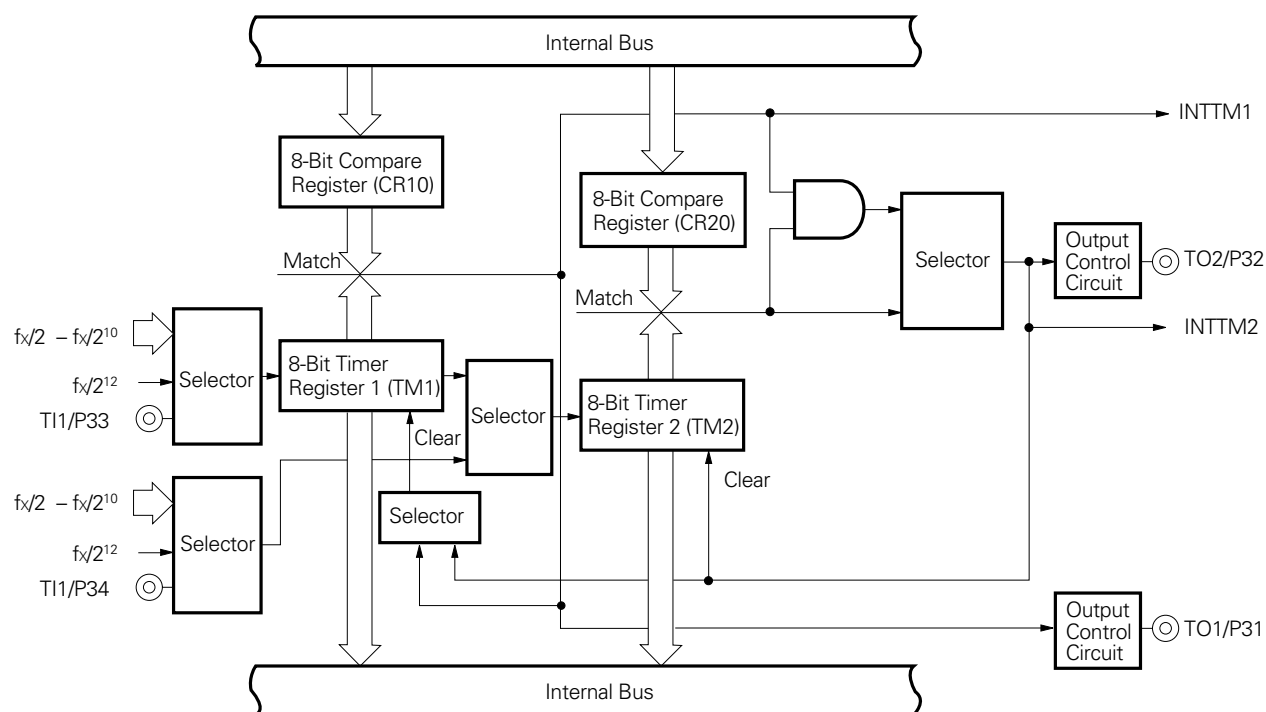


Fig. 5-3 Watch Timer Block Diagram

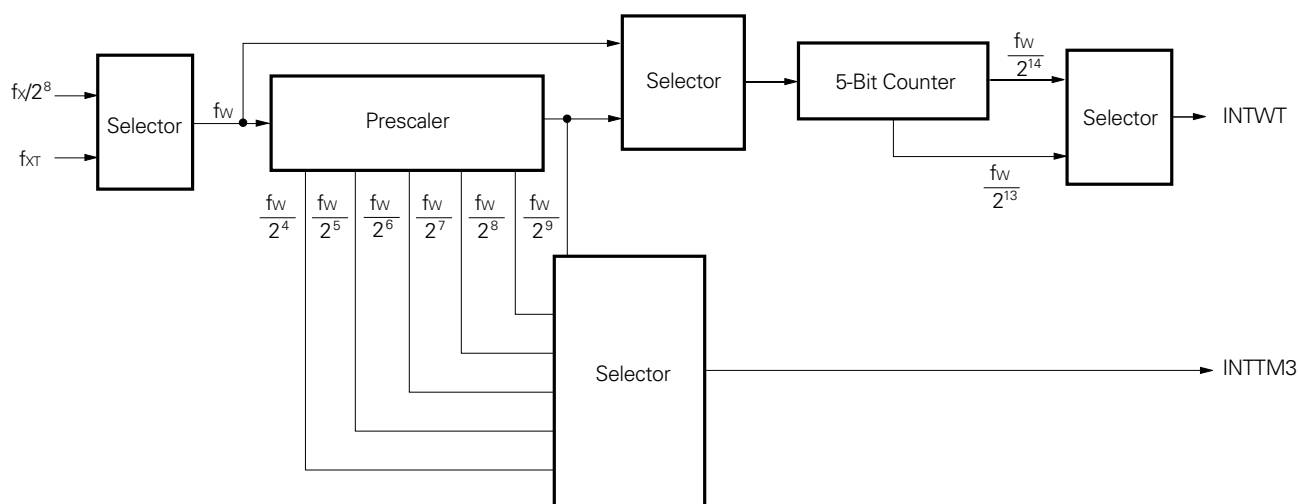
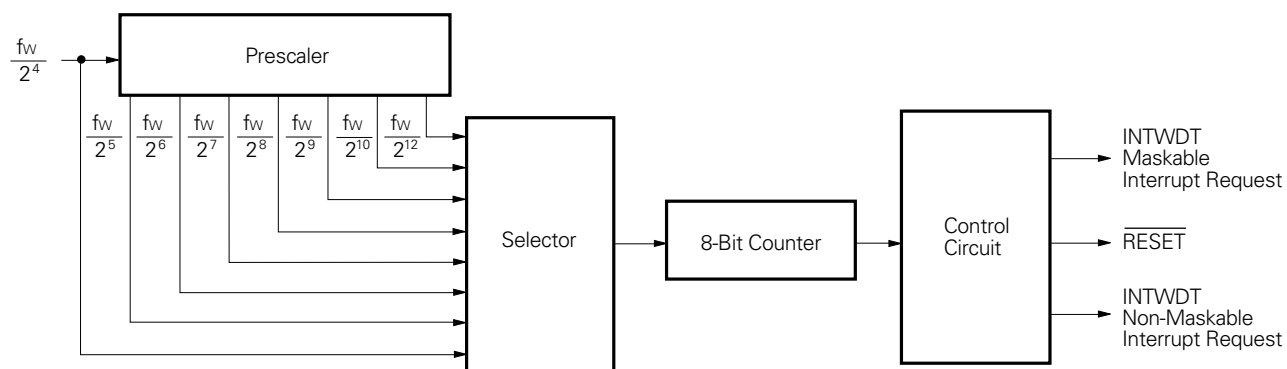


Fig. 5-4 Watchdog Timer Block Diagram

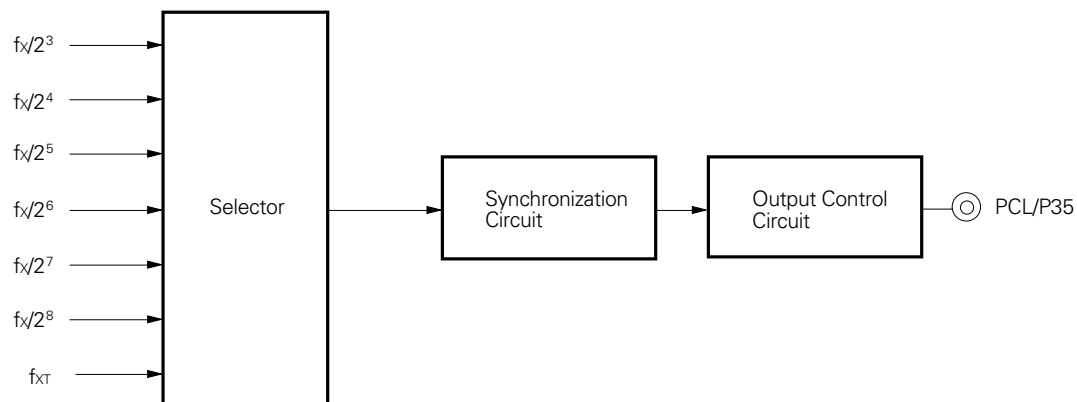


#### 5.4 CLOCK OUTPUT CONTROL CIRCUIT

The clock with the following frequencies can be output for clock output.

- 39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz (Main system clock: at 10.0 MHz operation)
- 32.768 kHz (Subsystem clock: at 32.768 kHz operation)

**Fig. 5-5 Clock Output Control Block Diagram**

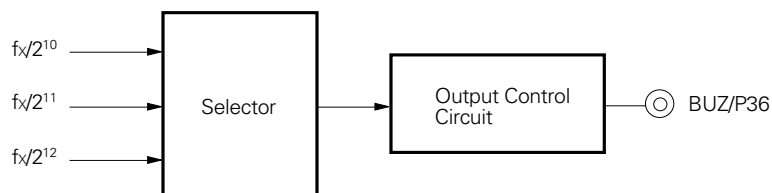


#### 5.5 BUZZER OUTPUT CONTROL CIRCUIT

The clock with the following frequencies can be output for buzzer output.

- 2.4 kHz/4.9 kHz/9.8 kHz (Main system clock: at 10.0 MHz operation)

**Fig. 5-6 Buzzer Output Control Block Diagram**



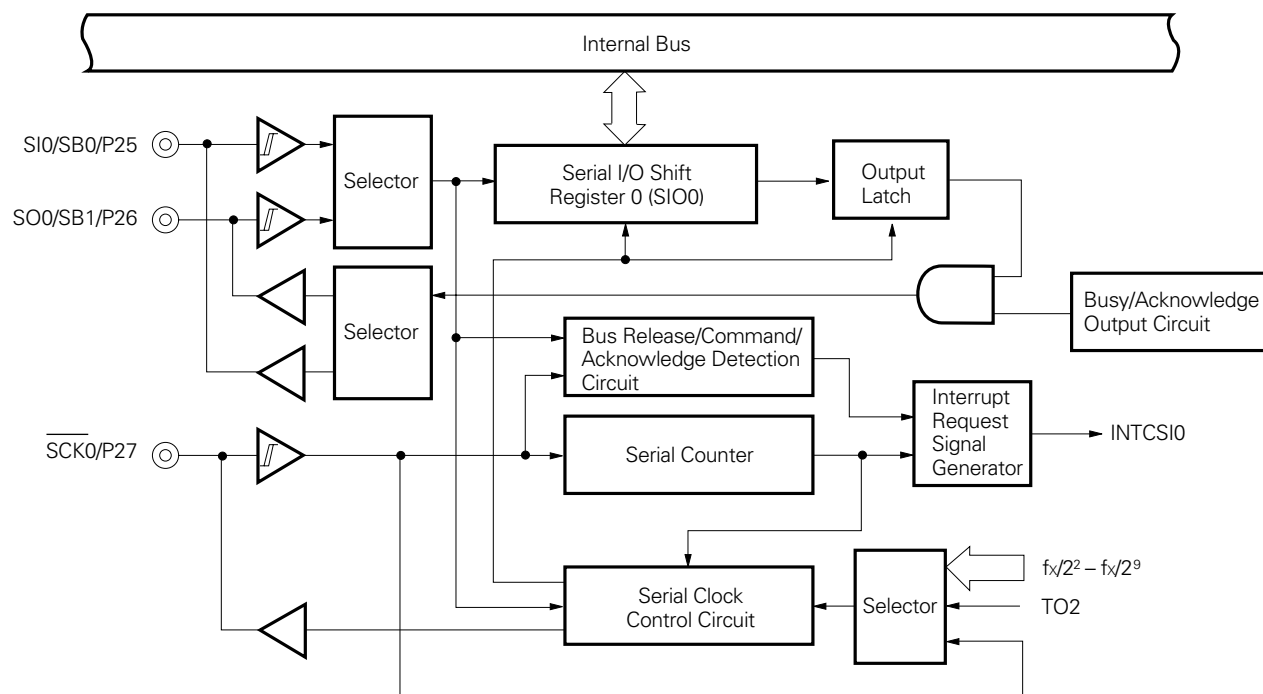
## 5.6 SERIAL INTERFACES

There is one on-chip clocked serial interface.

Serial Interface channel 0 has the following three modes.

- 3-wire serial I/O mode : MSB/LSB-first switchable
- SBI (Serial Bus Interface) mode : MSB-first
- 2-wire serial I/O mode : MSB-first

Fig. 5-7 Serial Interface Channel 0 Block Diagram



## 6. INTERRUPT FUNCTIONS AND DEST FUNCTIONS

### 6.1 INTERRUPT FUNCTIONS

There are 11 interrupt functions of 3 different kinds as shown below.

- Non-maskable interrupt : 1
- Maskable interrupt : 9
- Software interrupt : 1

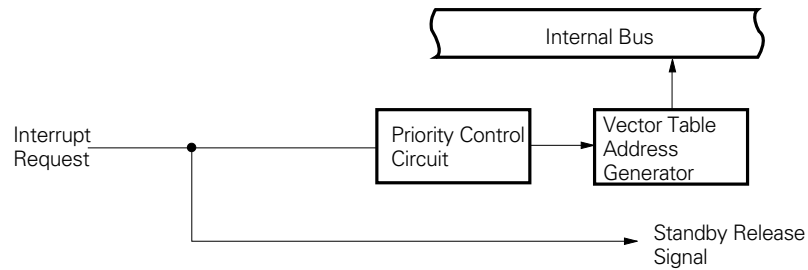
**Table 6-1 Interrupt Source List**

Interrupt Type	Default Priority *1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type *2
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (with non-maskable interrupt selected)	Internal	0004H	A
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer selected)			B
	1	INTP0	Pin input edge detection	External	0006H	C
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTCSI0	Serial interface channel 0 transfer end	Internal	000EH	B
	6	INTTM3	Reference time interval signal from watch timer		0012H	
	7	INTTM1	8-bit timer/event counter 1 match signal generation		0016H	
	8	INTTM2	8-bit timer/event counter 2 match signal generation		0018H	
Software	—	BRK	BRK instruction execution	Internal	003EH	E

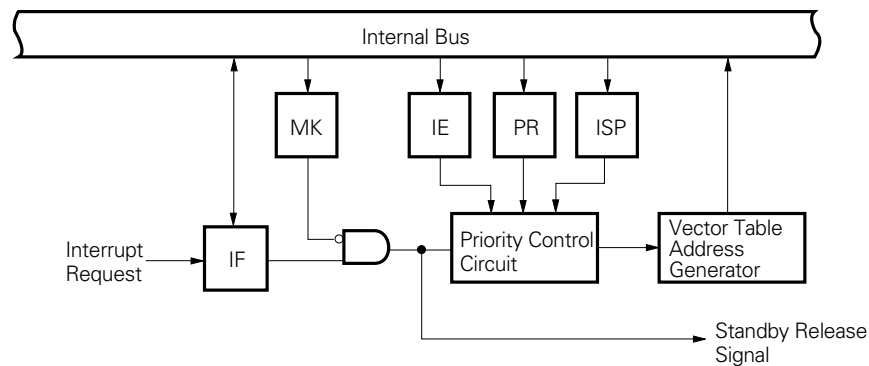
- \* 1. The default priority is the priority applicable when more priority than one maskable interrupt is generated. 0 is the highest and 11, the lowest.
2. Basic configuration types A to E correspond to (A) to (E) on the next page.

Fig. 6-1 Interrupt Function Basic Configuration (1/2)

(A) Internal Non-Maskable Interrupt



(B) Internal Maskable Interrupt



(C) External Maskable Interrupt (INTP0)

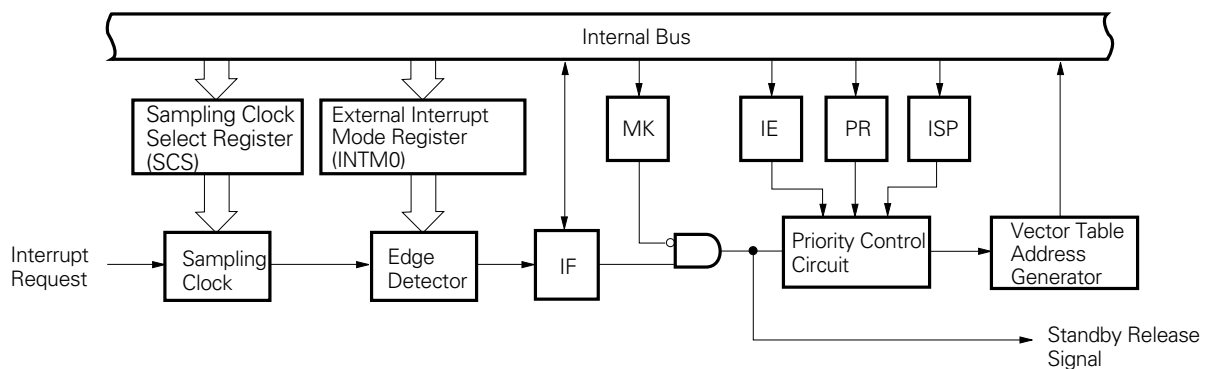
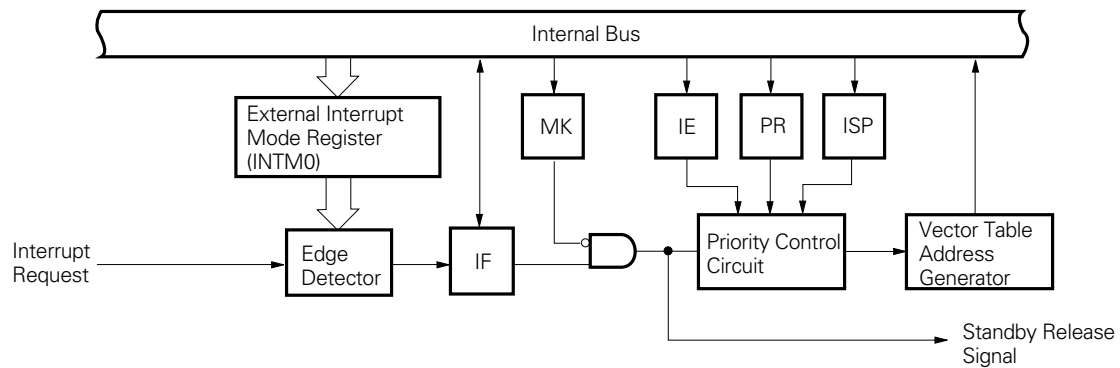
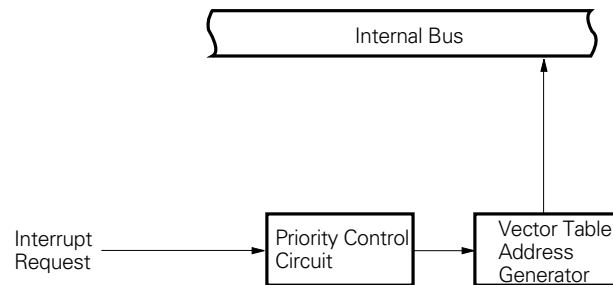


Fig. 6-1 Interrupt Function Basic Configuration (2/2)

## (D) External Maskable Interrupt (Except INTP0)



## (E) Software Interrupt



- Remarks**
1. IF : Interrupt request flag
  2. IE : Interrupt enable flag
  3. ISP : In-service priority flag
  4. MK : Interrupt mask flag
  5. PR : Priority specification flag



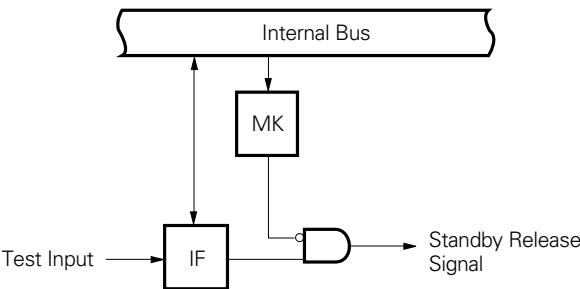
6.2 TEST FUNCTIONS

There are two test functions as shown in Table 6-2.

Table 6-2 Test Source List

Test Source		Internal/External
Name	Trigger	
INTWT	Watch timer overflow	Internal
NTPT4	Port 4 falling edge detection	External

Fig. 6-2 Test Function Basic Configuration



- Remarks**
- 1. IF : Test input flag
  - 2. MK : Test mask flag

## 7. EXTERNAL DEVICE EXPANSION FUNCTIONS

The external device expansion function is used to connect external devices to areas other than the internal ROM, RAM and SFR.

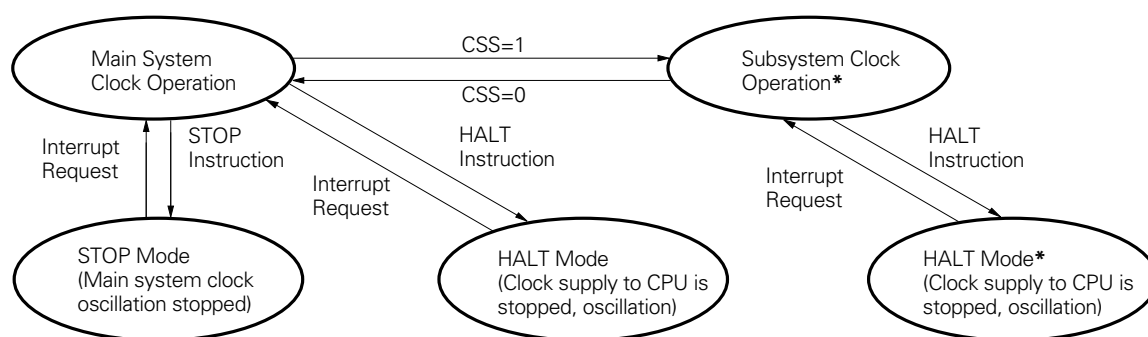
Ports 4 to 6 are used for connection with external devices.

## 8. STANDBY FUNCTIONS

There are the following two standby functions to reduce the current dissipation.

- **HALT mode** : The CPU operating clock is stopped. The average consumption current can be reduced by intermittent operation in combination with the normal operating mode.
- **STOP mode** : The main system clock oscillation is stopped. The whole operation by the main system clock is stopped, so that the system operates with ultra-low power consumption using only the sub-system clock.

**Fig. 8-1 Standby Functions**



- \* The power consumption can be reduced by stopping the main system clock. When the CPU is operating on the subsystem clock, set the MCC to stop the main system clock. The STOP instruction cannot be used.

**Caution** When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program by the program.

## 9. RESET FUNCTION

There are the following two reset methods.

- External reset input by  $\overline{\text{RESET}}$  pin.
- Internal reset by watchdog timer runaway time detection.

## 10. INSTRUCTION SET

### (1) 8-Bit Instruction

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand 1st Operand	#byte	A	r*	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	\$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
r1											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											

\* Except r = A

**(2) 16-Bit Instruction**

MOVW, XCHW ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd Operand 1st Operand	#word	AX	rp*	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW*						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

\* Only when rp = BC, DE, HL.

**(3) Bit Operation Instruction**

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd Operand 1st Operand	A.bit	sfr.bit	saddr.bit	PWS.bit	[HL].bit	CY	\$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

**(4) Call Instruction/Branch Instruction**

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

2nd Operand 1st Operand	AX	!addr16	!addr11	[addr5]	\$addr16
Basic instruction	BR	CALL, BR	CALLF	CALLT	BR, BC, BNC, BZ, BNZ
Compound instruction					BT, BF, BTCLR, DBNZ

**(5) Other Instruction**

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

## 11. ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings (T<sub>A</sub> = 25 °C)

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V <sub>DD</sub>			−0.3 to + 7.0	V
Input voltage	V <sub>I1</sub>	P00 to P04, P10 to P17, P20 to P27, P30 to P37 P40 to P47, P50 to P57, P64 to P67, X1, X2, XT2		−0.3 to V <sub>DD</sub> + 0.3	V
	V <sub>I2</sub>	P60 to P67	Open-drain	−0.3 to +16	V
Output voltage	V <sub>O</sub>			−0.3 to V <sub>DD</sub> + 0.3	V
Output current high	I <sub>OH</sub>	1 pin		−10	mA
		P10 to P17, P20 to P27, P30 to P37 total		−15	mA
		P01 to P03, P40 to P47, P50 to P57, P60 to P67 total		−15	mA
Output current low	I <sub>OL</sub> *	1 pin	Peak value	30	mA
			Effective value	15	mA
		P40 to P47, P50 to P55 total	Peak value	100	mA
			Effective value	70	mA
		P01 to P03, P56, P57, P60 to P67 total	Peak value	100	mA
			Effective value	70	mA
		P01 to P03, P64 to P67 total	Peak value	50	mA
			Effective value	20	mA
		P10 to P17, P20 to P27, P30 to P37 total	Peak value	50	mA
			Effective value	20	mA
Operating ambient temperature	T <sub>A</sub>			−40 to +85	°C
Storage temperature	T <sub>stg</sub>			−65 to +150	°C

\* Effective value should be calculated as follows:

$$[\text{Effective value}] = [\text{Peak value}] \times \sqrt{\text{duty}}$$

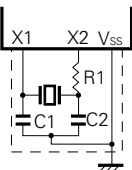
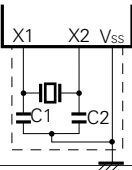
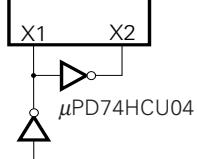
**Caution** Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

**Capacitance** ( $T_A = 25\text{ }^{\circ}\text{C}$ ,  $V_{DD} = V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	$C_{IN}$	$f=1\text{ MHz}$ Unmeasured pins returned to 0 V			15	pF
I/O capacitance	$C_{IO}$	$f=1\text{ MHz}$ Unmeasured pins returned to 0 V P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67			15	pF
		P60 to P63			20	pF

**Remark** The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

**Main System Clock Oscillation Circuit Characteristics** ( $T_A = -40\text{ to }+85\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 2.7\text{ to }6.0\text{ V}$ )

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency ( $f_x$ ) *1	$V_{DD}$ = Oscillator voltage range	1		10	MHz
		Oscillation stabilization time *2	After $V_{DD}$ reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency ( $f_x$ ) *1		1	8.38	10	MHz
		Oscillation stabilization time *2	$V_{DD} = 4.5\text{ to }6.0\text{ V}$			10 30	ms
External clock		X1 input frequency ( $f_x$ ) *1		1.0		10.0	MHz
		X1 input high/low level width ( $t_{XH}$ , $t_{XL}$ )		42.5		500	ns

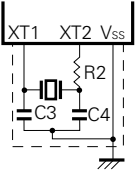
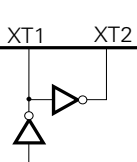
- \* 1. Indicates only oscillation circuit characteristics. Refer to “AC Characteristics” for instruction execution time.  
2. Time required to stabilize oscillation after reset or STOP mode release.

**Cautions** 1. When using the main system clock oscillator, wiring the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
- Wiring should not cross other signal lines.
- Wiring should not be placed close to a varying high current.
- The potential of the oscillator capacitor ground should be the same as VSS.
- Do not ground wiring to a ground pattern in which a high current flows.
- Do not fetch a signal from the oscillator.

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

**Subsystem Clock Oscillation Circuit Characteristics** ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 2.7$  to  $6.0$  V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (f <sub>XT</sub> ) *1		32	32.768	35	kHz
		Oscillation stabilization time *2	$V_{DD} = 4.5$ to $6.0$ V		1.2	2	s
						10	
External clock		XT1 input frequency (f <sub>XT</sub> ) *1		32		100	kHz
		XT1 input high/low level width (t <sub>XTH</sub> , t <sub>XTL</sub> )		5		15	$\mu$ s

- \* 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristics" for instruction execution time.  
 2. Time required to stabilize oscillation after  $V_{DD}$  reaches oscillator voltage MIN.

**Cautions** 1. When using the subsystem clock oscillator, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
  - Wiring should not cross other signal lines.
  - Wiring should not be placed close to a varying high current.
  - The potential of the oscillator capacitor ground should be the same as VSS.
  - Do not ground wiring to a ground pattern in which a high current flows.
  - Do not fetch a signal from the oscillator.
2. The subsystem clock oscillation circuit is a circuit with a low amplification level, more prone to misoperation due to noise than the main system clock. When using the subsystem clock, special care is needed regarding the wiring method.



## RECOMMENDED OSCILLATION CIRCUIT CONSTANT

### Main System Clock Ceramic Resonator (T<sub>A</sub> = -40 to +85 °C)

Manufacturer	Products	Frequency (MHz)	Recommended Oscillation Constant			Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Murata m.f.g.	CSB1000J	1.00	100	100	6.8	2.9	6.0
	CSB××××J	1.01-1.25	100	100	4.7	2.7	6.0
	CSA×.×××MK	1.26-1.79	100	100	0	2.7	6.0
	CSA×.××MG	1.80-2.44	100	100	0	2.7	6.0
	CST×.××MG		On-chip	On-chip	0	2.7	6.0
	CSA×.××MG	2.45-4.18	30	30	0	2.7	6.0
	CST×.××MGW		On-chip	On-chip	0	2.7	6.0
	CSA×.××MG	4.19-6.00	30	30	0	2.7	6.0
	CST×.××MGW		On-chip	On-chip	0	2.7	6.0
	CSA×.××MT	6.01-10.0	30	30	0	2.9	6.0
	CST×.××MTW		On-chip	On-chip	0	2.9	6.0
Kyocera	KBR-4.19MWS	4.19	—	—	—	2.7	6.0
	KBR-4.19MKS		—	—	—	2.7	6.0
	KBR-4.19MSA	4.19	33	33	—	2.7	6.0
	PBRC4.19A		33	33	—	2.8	6.0
	KBR-10.0M	10.0	33	33	—	2.8	6.0
	KBR-1000F	1.00	100	100	2.2	2.7	6.0
	KBR-1000Y		100	100	2.2	2.7	6.0

**Remark** ××××, ×.×××, ×.×× indicates frequency.

### Subsystem Clock: Crystal Resonator (T<sub>A</sub> = -40 to +60 °C)

Manufacturer	Products	Frequency (MHz)	Recommended Circuit Constant			Oscillation Voltage Range	
			C3 (pF)	C4 (pF)	R2 (kΩ)	MIN. (V)	MAX. (V)
Daishinku corp.	DT-38 (1TA632E00, Load capacitance 6.3pF)	32.768	8	8	100	2.7	6.0

**Caution** Regarding the oscillator circuit constant, operation is guaranteed, but reliability is not guaranteed. Customers who require high reliability should directly consult the resonator manufacturer.

**DC Characteristics** ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 2.7$  to  $6.0$  V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V <sub>IH1</sub>	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67		0.7 V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH2</sub>	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$		0.8 V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH3</sub>	P60 to P63	Open-drain	0.7 V <sub>DD</sub>		15	V
	V <sub>IH4</sub>	X1, X2		V <sub>DD</sub> -0.5		V <sub>DD</sub>	V
	V <sub>IH5</sub>	XT1/P04, XT2	V <sub>DD</sub> = 4.5 to 6.0 V	V <sub>DD</sub> -0.5		V <sub>DD</sub>	V
				V <sub>DD</sub> -0.3		V <sub>DD</sub>	V
Input voltage low	V <sub>IL1</sub>	P10 to P17, P21, P23, P30 to P32, P35 to P37 P40 to P47, P50 to P57, P64 to P67		0		0.3 V <sub>DD</sub>	V
	V <sub>IL2</sub>	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$		0		0.2 V <sub>DD</sub>	V
	V <sub>IL3</sub>	P60 to P63	V <sub>DD</sub> = 4.5 to 6.0 V	0		0.3 V <sub>DD</sub>	V
				0		0.2 V <sub>DD</sub>	V
	V <sub>IL4</sub>	X1, X2		0		0.4	V
	V <sub>IL5</sub>	XT1/P04, XT2	V <sub>DD</sub> = 4.5 to 6.0 V	0		0.4	V
				0		0.3	V
Output voltage high	V <sub>OH1</sub>	V <sub>DD</sub> = 4.5 to 6.0 V, I <sub>OH</sub> = -1 mA		V <sub>DD</sub> -1.0			V
		I <sub>OH</sub> = -100 μA		V <sub>DD</sub> -0.5			V
Output voltage low	V <sub>OL1</sub>	P50 to P57, P60 to P63	V <sub>DD</sub> = 4.5 to 6.0 V, I <sub>OL</sub> = 15 mA		0.4	2.0	V
		P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67	V <sub>DD</sub> = 4.5 to 6.0 V, I <sub>OL</sub> = 1.6 mA			0.4	V
	V <sub>OL2</sub>	SB0, SB1, $\overline{\text{SCK0}}$	V <sub>DD</sub> = 4.5 to 6.0 V, open-drain pulled-up (R = 1 KΩ )			0.2 V <sub>DD</sub>	V
	V <sub>OL3</sub>	I <sub>OL</sub> = 400 μA				0.5	V
Input leakage current high	I <sub>LIH1</sub>	V <sub>IN</sub> = V <sub>DD</sub>	P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, $\overline{\text{RESET}}$			3	μA
	I <sub>LIH2</sub>		X1, X2, XT1/P04, XT2			20	μA
	I <sub>LIH3</sub>	V <sub>IN</sub> = 15 V	P60 to P63			80	μA
Input leakage current high	I <sub>LIL1</sub>	V <sub>IN</sub> = 0 V	P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, $\overline{\text{RESET}}$			-3	μA
	I <sub>LIL2</sub>		X1, X2, XT1/P04, XT2			-20	μA
	I <sub>LIL3</sub>		P60 to P63	*1		-200	μA
				Other than above		-3 <sup>+2</sup>	μA

- \* 1. When memory expansion mode is used by the memory expansion mode register (MM) with no on-chip pull-up resistor by mask option.  
 2. When pull-up resistors are not used (specified by mask option), the low-level input leakage current increases with  $-200$   $\mu$ A (MAX.) under either of the following conditions.  
 ① When the external device expansion function is used and a low level is input to the pin.  
 ② During the 3-clock period when a read instruction is executed on port 6 (P6) and the port mode register (PM6).

**Remark** The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

**DC Characteristics** ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 2.7$  to  $6.0$  V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Output leakage current high	I <sub>LOH1</sub>	$V_{OUT} = V_{DD}$				3	μA
Output leakage current low	I <sub>LOL</sub>	$V_{OUT} = 0$ V				−3	μA
Mask option pull-up resistor	R <sub>1</sub>	$V_{IN} = 0$ V, P60 to P63		20	40	90	kΩ
Software pull-up resistor	R <sub>2</sub>	$V_{IN} = 0$ V, P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67	$4.5 \text{ V} \leq V_{DD} < 6.0 \text{ V}$	15	40	90	kΩ
			$2.7 \text{ V} \leq V_{DD} < 4.5 \text{ V}$	20		500	kΩ
Power supply current *3	I <sub>DD1</sub>	8.38 MHz Crystal oscillation operating mode	$V_{DD} = 5.0 \text{ V} \pm 10\%$ *1		7.5	22.5	mA
			$V_{DD} = 3.0 \text{ V} \pm 10\%$ *2		0.8	2.4	mA
	I <sub>DD2</sub>	8.38 MHz Crystal oscillation HALT mode	$V_{DD} = 5.0 \text{ V} \pm 10\%$		1.4	4.2	mA
			$V_{DD} = 3.0 \text{ V} \pm 10\%$		550	1650	μA
	I <sub>DD3</sub>	32.768 kHz Crystal oscillation operating mode	$V_{DD} = 5.0 \text{ V} \pm 10\%$		60	120	μA
			$V_{DD} = 3.0 \text{ V} \pm 10\%$		35	70	μA
	I <sub>DD4</sub>	32.768 kHz Crystal oscillation HALT mode	$V_{DD} = 5.0 \text{ V} \pm 10\%$		25	50	μA
			$V_{DD} = 3.0 \text{ V} \pm 10\%$		5	10	μA
	I <sub>DD5</sub>	XT1 = 0 V STOP mode When feedback resistor is used	$V_{DD} = 5.0 \text{ V} \pm 10\%$		1	20	μA
			$V_{DD} = 3.0 \text{ V} \pm 10\%$		0.5	10	μA
	I <sub>DD6</sub>	XT1 = 0 V STOP mode When feedback resistor is unused	$V_{DD} = 5.0 \text{ V} \pm 10\%$		0.1	20	μA
			$V_{DD} = 3.0 \text{ V} \pm 10\%$		0.05	10	μA

- \* 1. Operating in high-speed mode (when set the processor clock control register to 00H).  
 2. Operating in low-speed mode (when set the processor clock control register to 04H).  
 3. Port current are excluded.

**Remark** The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

**AC Characteristics** ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 2.7$  to  $6.0$  V)

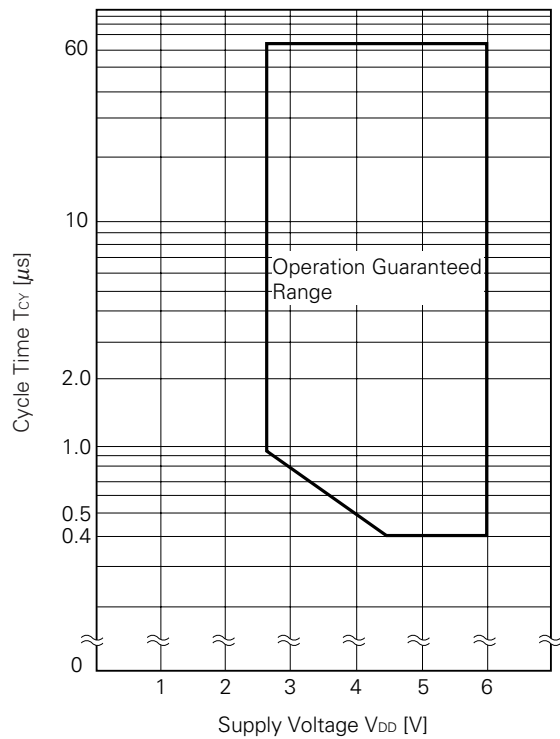
**(1) Basic Operation**

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	$T_{CY}$	Operating on main system clock	0.4		64	$\mu s$
		$V_{DD} = 4.5$ to $6.0$ V	0.96		64	$\mu s$
		Operating on subsystem clock	40	122	125	$\mu s$
TI input frequency	$f_{TI}$	$V_{DD} = 4.5$ to $6.0$ V	0		4	MHz
			0		275	kHz
TI input high/ low-level width	$t_{TIH}$ $t_{TIL}$	$V_{DD} = 4.5$ to $6.0$ V	100			ns
			1.8			$\mu s$
Interrupt input high/low-level width	$t_{INTH}$ $t_{INTL}$	INTP0	$8/f_{sam}^*$			$\mu s$
		INTP1 to INTP3	10			$\mu s$
		KR0 to KR7	10			$\mu s$
RESET low level width	$t_{RSL}$		10			$\mu s$

\* In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register, selection of  $f_{sam}$  is possible between  $f_X/2^{N+1}$ ,  $f_X/64$  and  $f_X/128$  (when  $N = 0$  to  $4$ ).

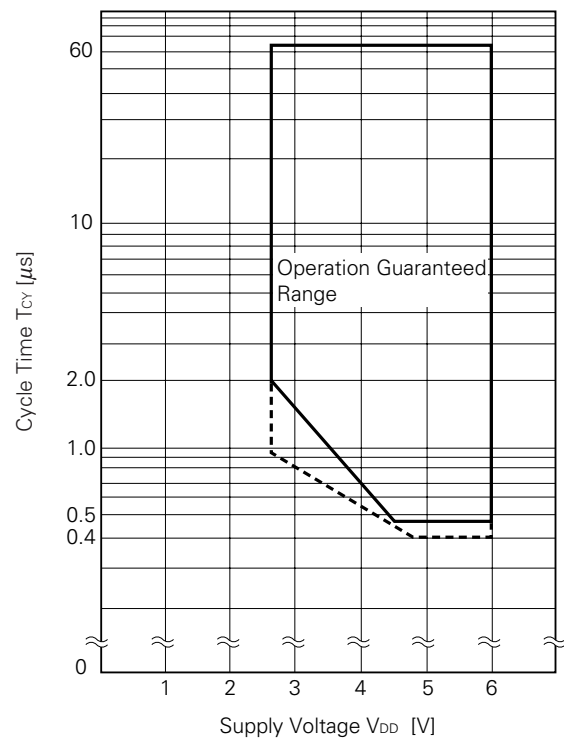
**μPD78001B(A), 78002B(A)**

**$T_{CY}$  vs  $V_{DD}$  (At main system clock operation)**



**μPD78P014 (Reference)**

**$T_{CY}$  vs  $V_{DD}$  (At main system clock operation)**



**Remark**      - - - - - indicates  $T_A = -40$  to  $+40$  °C  
                     ——— indicates  $T_A = -40$  to  $+85$  °C

**Caution**    The operation guaranteed range of the μPD78001B(A), and 78002B(A) differs from that of the μPD78P014.

(2) Read/Write Operation ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 2.7$  to  $6.0$  V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	tASTH		0.5tcy		ns
Address setup time	tADS		0.5tcy-30		ns
Address hold time	tADH	Load resistor $\geq 5$ k $\Omega$	10		ns
Data input time from address	tADD1			(2+2n)tcy-50	ns
	tADD2		5	(3+2n)tcy-100	ns
Data input time from $\overline{RD}\downarrow$	trDD1			(1+2n)tcy-25	ns
	trDD2			(2.5+2n)tcy-100	ns
Read data hold time	trDH		0		ns
$\overline{RD}$ low-level width	trDL1		(1.5+2n)tcy-20		ns
	trDL2		(2.5+2n)tcy-20		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	trDWT1			0.5tcy	ns
	trDWT2			1.5tcy	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	tWRWT			0.5tcy	ns
$\overline{WAIT}$ low-level width	twTL		(0.5+2n)tcy + 10	(2+2n)tcy	ns
Write data setup time	twDS		100		ns
Write data hold time	twDH		5		ns
$\overline{WR}$ low-level width	twRL1		(2.5+2n)tcy -20		ns
$\overline{RD}\downarrow$ delay time from ASTB $\downarrow$	tASTRD		0.5tcy-30		ns
$\overline{WR}\downarrow$ delay time from ASTB $\downarrow$	tASTWR		1.5tcy -30		ns
ASTB $\uparrow$ delay time from $\overline{RD}\uparrow$ in external fetch	trDAST		tcy-10	tcy+40	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	trDADH		tcy	tcy+50	ns
Write data output time from $\overline{RD}\uparrow$	trDWD		10		ns
$\overline{WR}\downarrow$ delay time from write data	twDWR	$V_{DD} = 4.5$ to $6.0$ V	0.5tcy-120	0.5tcy	ns
			0.5tcy-170	0.5tcy	ns
Address hold time from $\overline{WR}\uparrow$	twRADH	$V_{DD} = 4.5$ to $6.0$ V	tcy	tcy+60	ns
			tcy	tcy+100	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	twTRD		0.5tcy	2.5tcy+80	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	twTWR		0.5tcy	2.5tcy+80	ns

- Remarks**
1. tcy = Tcy/4
  2. n indicates number of waits.
  3. CL = 100 pF (CL indicates load capacitance of P40/AD0 to P47/AD7, P50/A8 to P57/A15, P64/ $\overline{RD}$ , P65/ $\overline{WR}$ , P66/ $\overline{WAIT}$ , P67/ASTB pins).

(3) Serial Interface ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 2.7$  to  $6.0$  V)

(a) 3-wire serial I/O mode ( $\overline{SCK}$ ... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	tkCY1	$V_{DD} = 4.5$ to $6.0$ V		800			ns
				3200			ns
$\overline{SCK}$ high/low-level width	tkH1	$V_{DD} = 4.5$ to $6.0$ V		tkCY1/2-50			ns
	tkL1			tkCY1/2-150			ns
SI setup time (to $\overline{SCK}\uparrow$ )	tsIK1			100			ns
SI hold time (from $\overline{SCK}\uparrow$ )	tkSI1			400			ns
SO output delay time from $\overline{SCK}\downarrow$	tkSO1	C = 100 pF*	$V_{DD} = 4.5$ to $6.0$ V			300	ns
						1000	ns

\* C is the load capacitance of SO output line.

(b) 3-wire serial I/O mode ( $\overline{SCK}$ ... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	tkCY2	$V_{DD} = 4.5$ to $6.0$ V		800			ns
				3200			ns
$\overline{SCK}$ high/low-level width	tkH2	$V_{DD} = 4.5$ to $6.0$ V		400			ns
	tkL2			1600			ns
SI setup time (to $\overline{SCK}\uparrow$ )	tsIK2			100			ns
SI hold time (from $\overline{SCK}\uparrow$ )	tkSI2			400			ns
SO output delay time from $\overline{SCK}\downarrow$	tkSO2	C = 100 pF*	$V_{DD} = 4.5$ to $6.0$ V			300	ns
						1000	ns
$\overline{SCK}$ rise, fall time	tr2	When external device expansion function is used				160	ns
	tf2	When external device expansion function is not used				1000	ns

\* C is the load capacitance of SO output line.

(c) SBI mode ( $\overline{\text{SCK}}$ ... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	tkCY3	V <sub>DD</sub> = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{\text{SCK}}$ high/low-level width	tkH3 tkL3	V <sub>DD</sub> = 4.5 to 6.0 V		tkCY3/2-50			ns
				tkCY3/2-150			ns
SB0, SB1 setup time (to $\overline{\text{SCK}}\uparrow$ )	tsIK3	V <sub>DD</sub> = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time from $\overline{\text{SCK}}\downarrow$	tkSI3			tkCY3/2			ns
SB0, SB1 output delay time (from $\overline{\text{SCK}}\uparrow$ )	tkSO3	R = 1 kΩ ,	V <sub>DD</sub> = 4.5 to 6.0 V	0		250	ns
		C = 100 pF*		0		1000	ns
SB0, SB1↓ from $\overline{\text{SCK}}\uparrow$	tkSB			tkCY3			ns
$\overline{\text{SCK}}\downarrow$ from SB0, SB1↓	tsBK			tkCY3			ns
SB0, SB1 high-level width	tsBH			tkCY3			ns
SB0, SB1 low-level width	tsBL			tkCY3			ns

\* R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

(d) SBI mode ( $\overline{\text{SCK}}$ ... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	tkCY4	V <sub>DD</sub> = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{\text{SCK}}$ high/low-level width	tkH4 tkL4	V <sub>DD</sub> = 4.5 to 6.0 V		400			ns
				1600			ns
SB0, SB1 setup time (to $\overline{\text{SCK}}\uparrow$ )	tsIK4	V <sub>DD</sub> = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{\text{SCK}}\downarrow$ )	tkSI4			tkCY4/2			ns
SB0, SB1 output delay time from $\overline{\text{SCK}}\uparrow$	tkSO4	R = 1 kΩ ,	V <sub>DD</sub> = 4.5 to 6.0 V	0		300	ns
		C = 100 pF*		0		1000	ns
SB0, SB1↓ from $\overline{\text{SCK}}\uparrow$	tkSB			tkCY4			ns
$\overline{\text{SCK}}\downarrow$ from SB0, SB1↓	tsBK			tkCY4			ns
SB0, SB1 high-level width	tsBH			tkCY4			ns
SB0, SB1 low-level width	tsBL			tkCY4			ns
$\overline{\text{SCK}}$ rise, fall time	tr4	When external device expansion function is used				160	ns
	tf4	When external device expansion function is not used				1000	ns

\* R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

**(e) 2-wire serial I/O mode ( $\overline{\text{SCK}}$ ... Internal clock output)**

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	tkCY5	$V_{DD} = 4.5 \text{ to } 6.0 \text{ V}$		1600			ns
				3800			ns
$\overline{\text{SCK}}$ high-level width	tkH5	$R = 1 \text{ k}\Omega, C = 100 \text{ pF}^*$		tkCY5/2-50			ns
$\overline{\text{SCK}}$ low-level width	tkL5			tkCY5/2-50			ns
SB0, SB1 setup time (to $\overline{\text{SCK}}\uparrow$ )	tsIK5			300			ns
SB0, SB1 hold time (from $\overline{\text{SCK}}\uparrow$ )	tkSI5			600			ns
SB0, SB1 output delay time from $\overline{\text{SCK}}\downarrow$	tkSO5	$R = 1 \text{ k}\Omega,$ $C = 100 \text{ pF}^*$	$V_{DD} = 4.5 \text{ to } 6.0 \text{ V}$	0		250	ns
				0		1000	ns

\* R and C are the load resistors and load capacitance of the  $\overline{\text{SCK0}}$ , SB0 and SB1 output line.

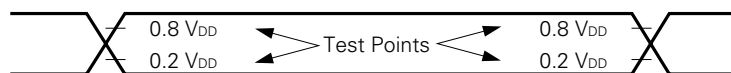
**(f) 2-wire serial I/O mode ( $\overline{\text{SCK}}$ ... External clock input)**

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK}}$ cycle time	tkCY6	$V_{DD} = 4.5 \text{ to } 6.0 \text{ V}$		1600			ns
				3800			ns
$\overline{\text{SCK}}$ high-level width	tkH6			650			ns
$\overline{\text{SCK}}$ low-level width	tkL6			800			ns
SB0, SB1 setup time (to $\overline{\text{SCK}}\uparrow$ )	tsIK6			100			ns
SB0, SB1 hold time (from $\overline{\text{SCK}}\uparrow$ )	tkSI6			tkCY6/2			ns
SB0, SB1 output delay time from $\overline{\text{SCK}}\downarrow$	tkSO6	$R = 1 \text{ k}\Omega,$ $C = 100 \text{ pF}^*$	$V_{DD} = 4.5 \text{ to } 6.0 \text{ V}$	0		300	ns
				0		1000	ns
$\overline{\text{SCK}}$ rise, fall time	tr6	When external device expansion function is used				160	ns
	tf6	When external device expansion function is not used				1000	ns

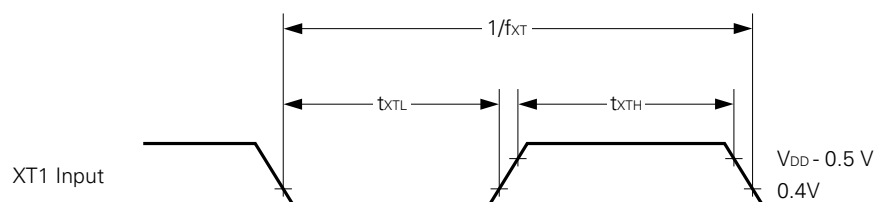
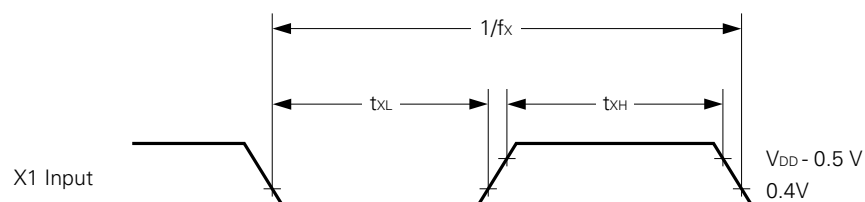
\* R and C are the load resistors and load capacitance of the  $\overline{\text{SCK0}}$ , SB0 and SB1 output line.



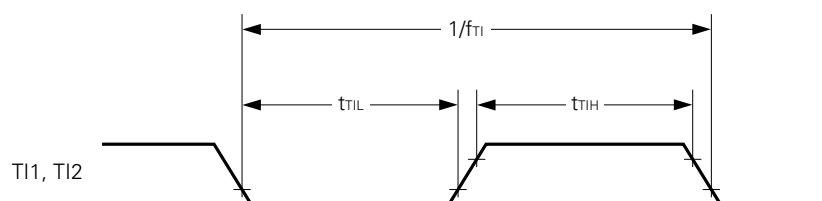
# AC Timing Test Point (Excluding X1, XT1 Input)

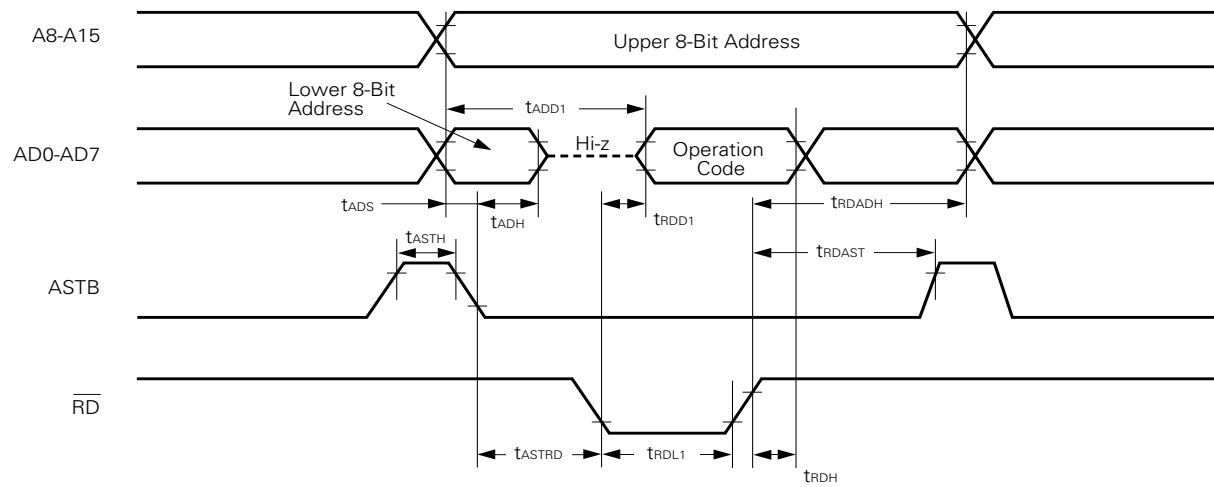
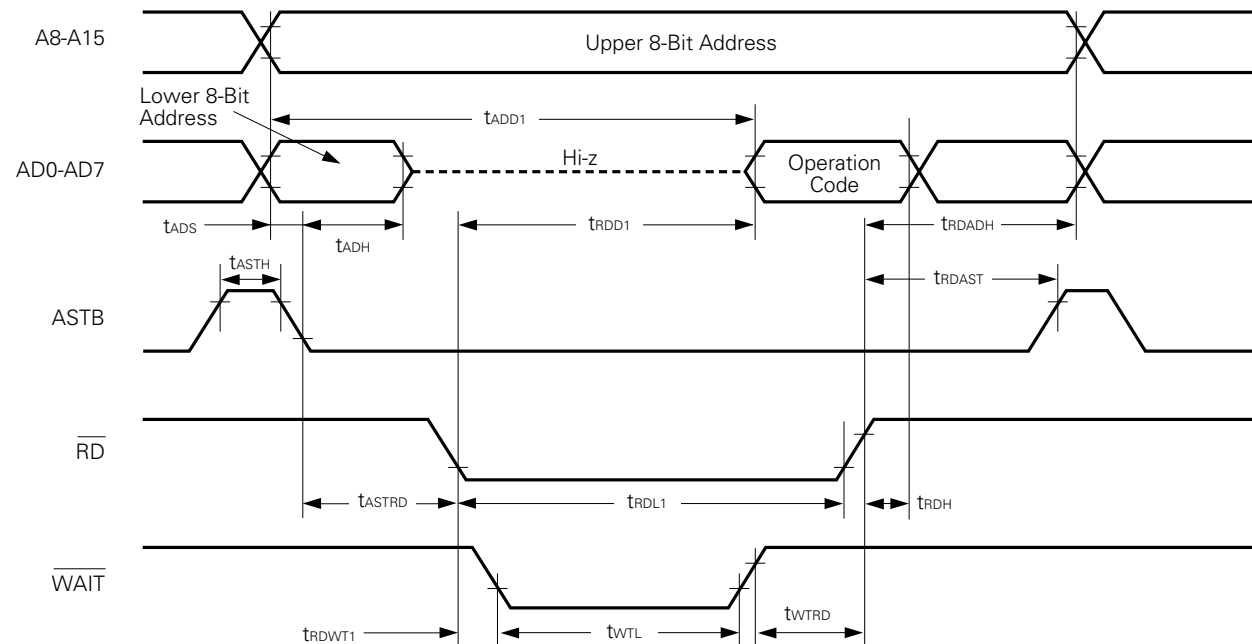


## Clock Timing

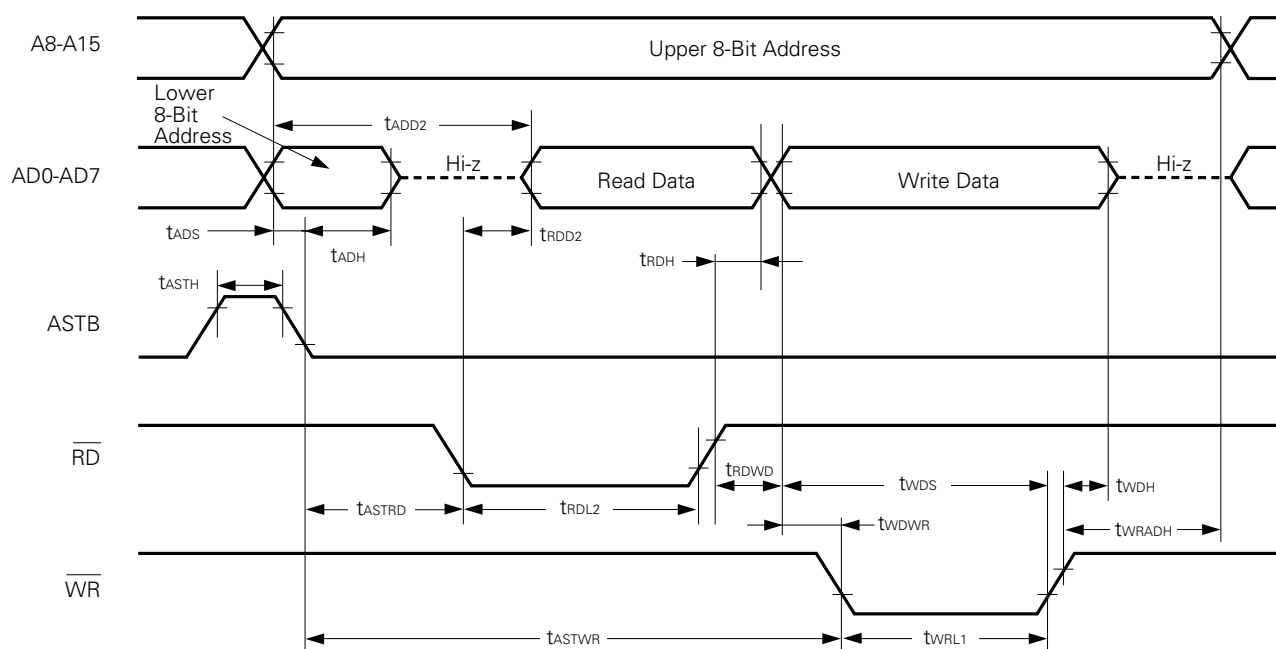


## TI Timing

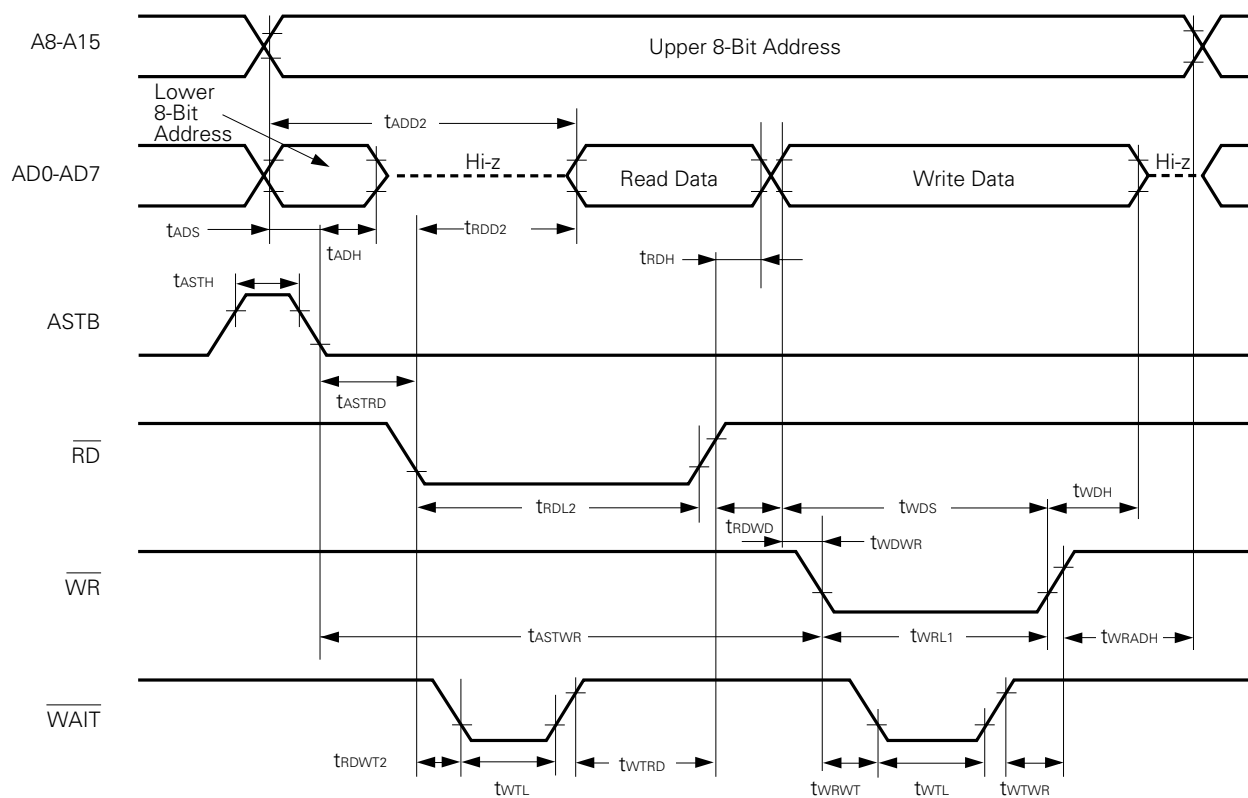


**Read/Write Operation****External fetch (no wait):****External fetch (wait insertion):**

**External data access (No wait):**

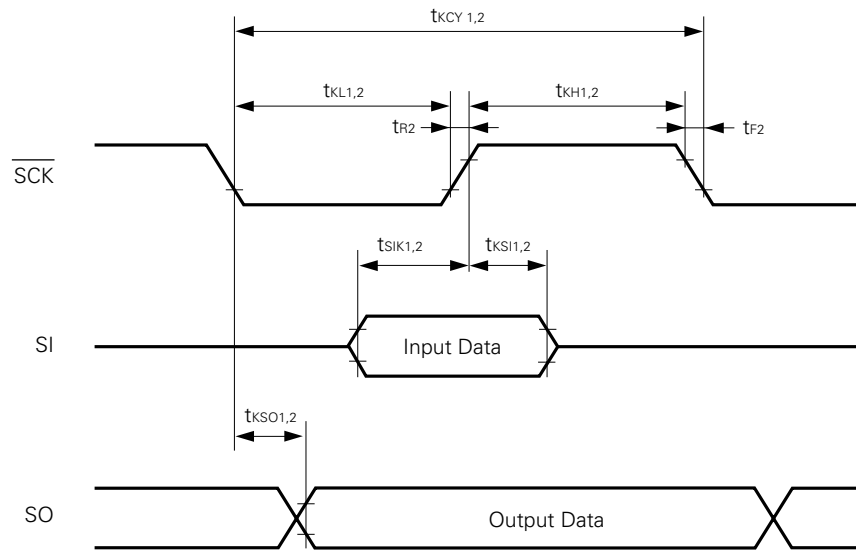


**External data access (Wait insertion):**

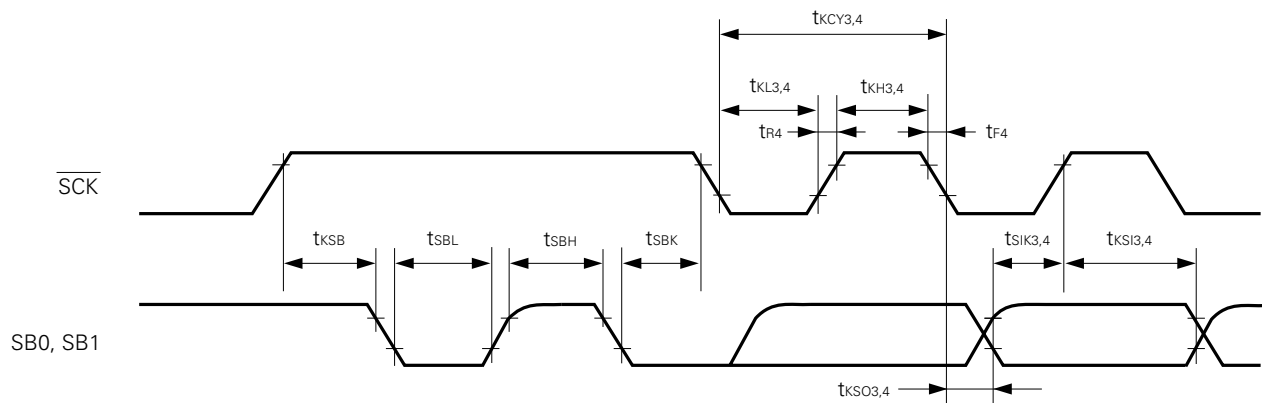


## Serial Transfer Timing

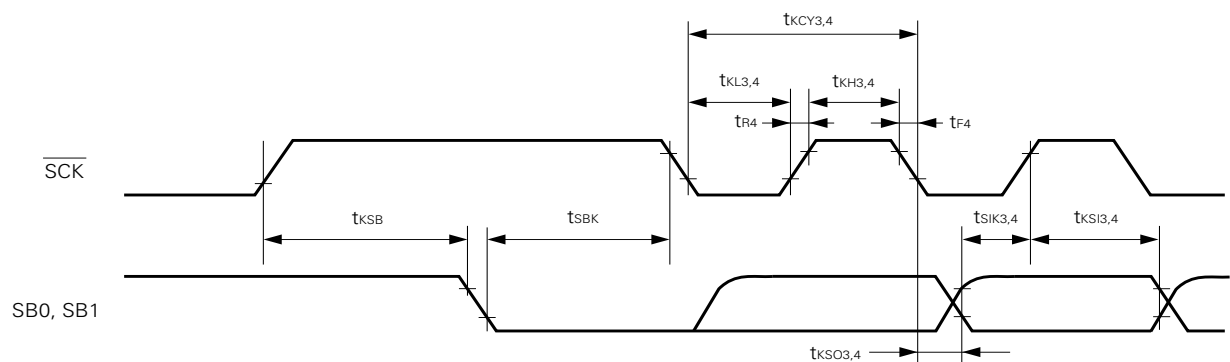
### 3-wire serial I/O mode:



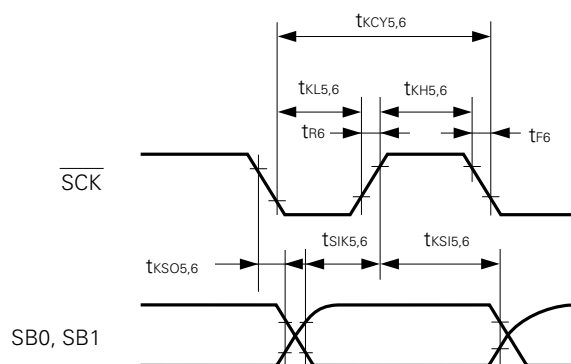
### SBI mode (Bus release signal transfer):



### SBI mode (Command signal transfer):



2-wire serial I/O mode:

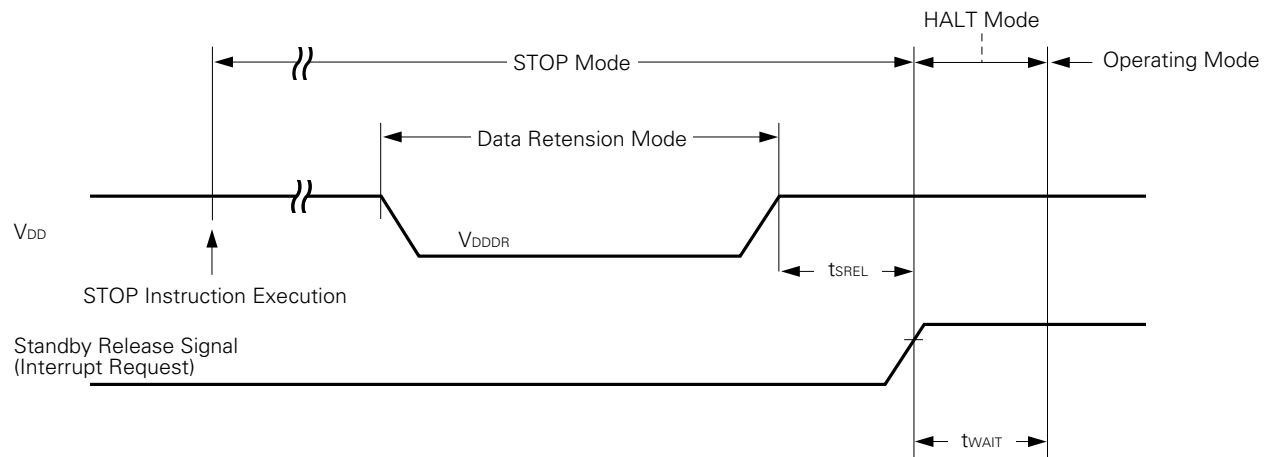


**Data Memory Stop Mode Low Supply Voltage Data Retention Characteristics (T<sub>A</sub> = -40 to +85 °C)**

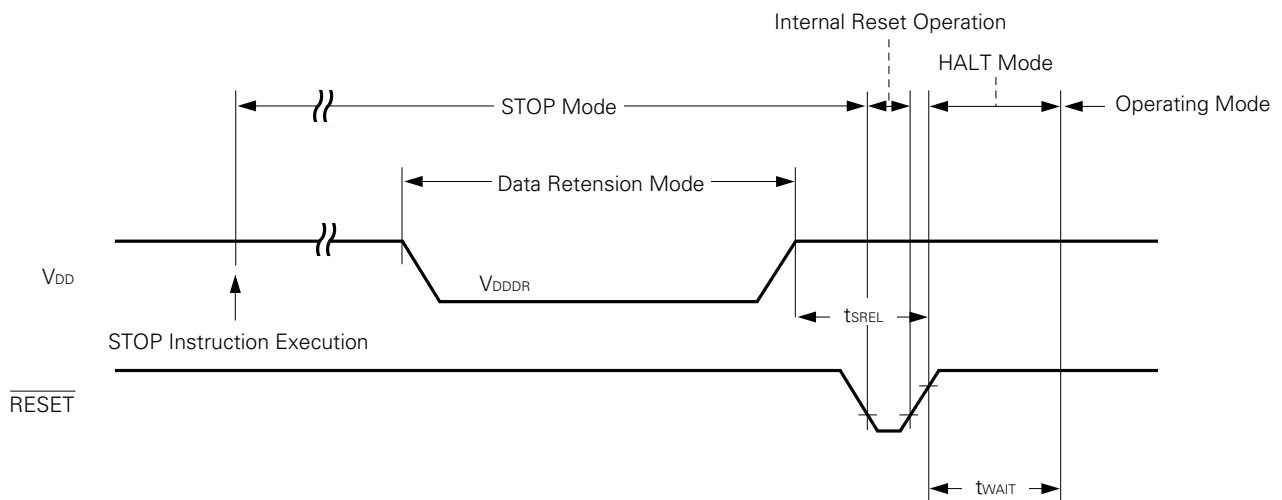
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V <sub>DDDR</sub>		2.0		6.0	V
Data retention supply current	I <sub>DDDR</sub>	V <sub>DDDR</sub> = 2.0 V Subsystem clock stop and feed-back resistor disconnected		0.1	10	μA
Release signal set time	t <sub>SREL</sub>		0			μs
Oscillation stabilization wait time	t <sub>WAIT</sub>	Release by <u>RESET</u>		2 <sup>18</sup> /f <sub>x</sub>		μs
		Release by interrupt		*		μs

\* In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register, selection of 2<sup>13</sup>/f<sub>x</sub> and 2<sup>15</sup>/f<sub>x</sub> to 2<sup>18</sup>/f<sub>x</sub> is possible.

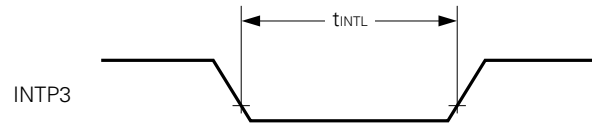
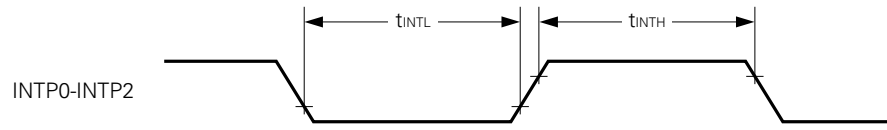
**Data Retention Timing (STOP Mode Release by RESET)**



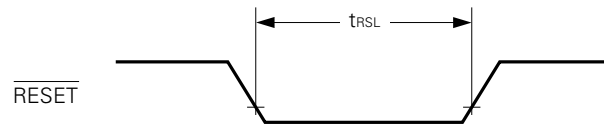
**Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)**



### Interrupt Input Timing

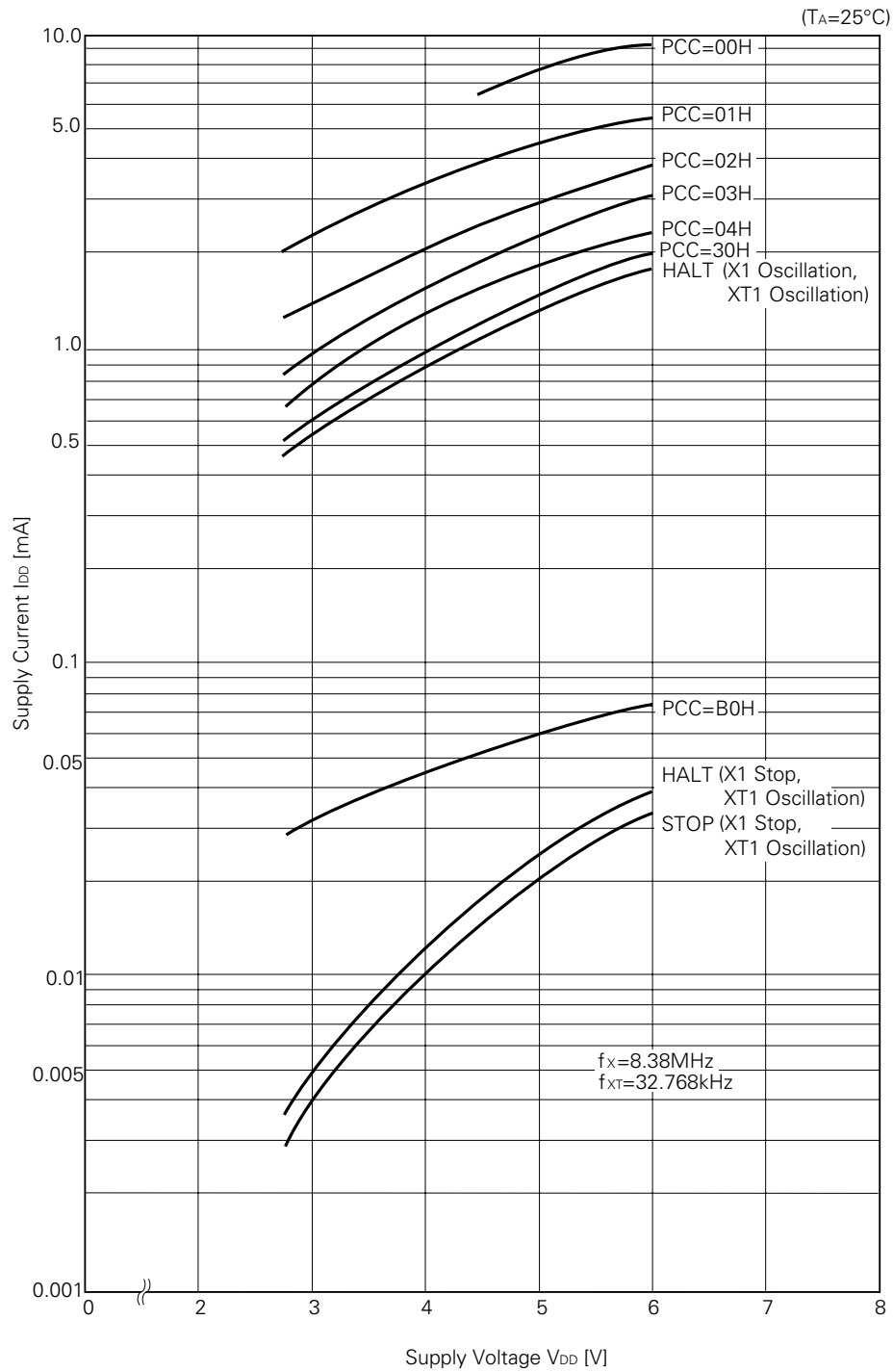


### $\overline{\text{RESET}}$ Input Timing

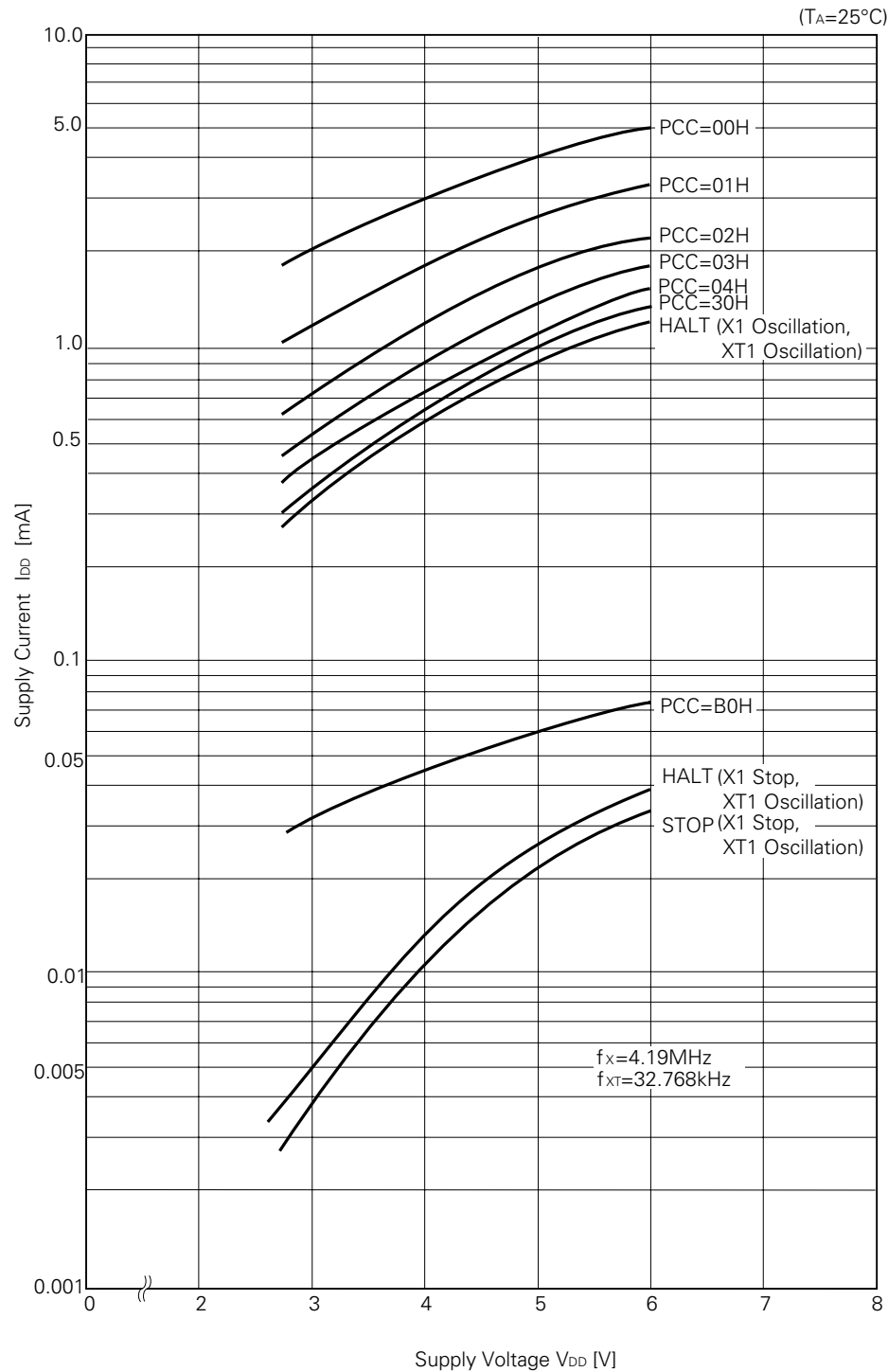


## 12. CHARACTERISTIC CURVE (REFERENCE VALUES)

$I_{DD}$  vs  $V_{DD}$  (Main System Clock : 8.38 MHz)

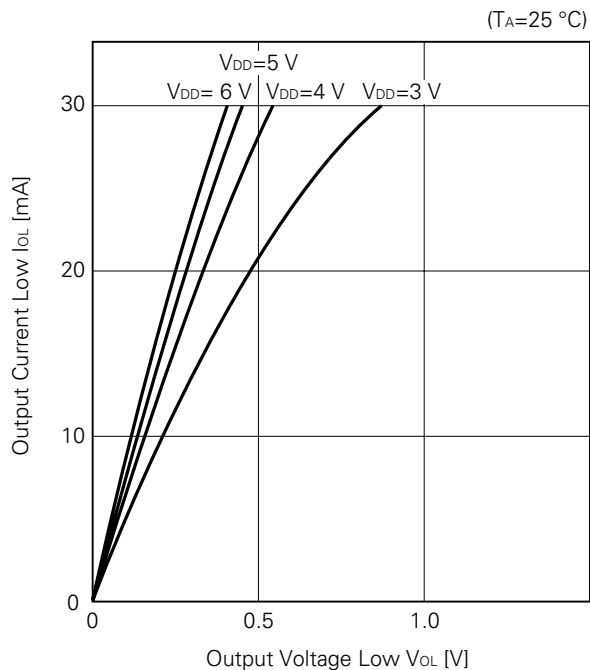




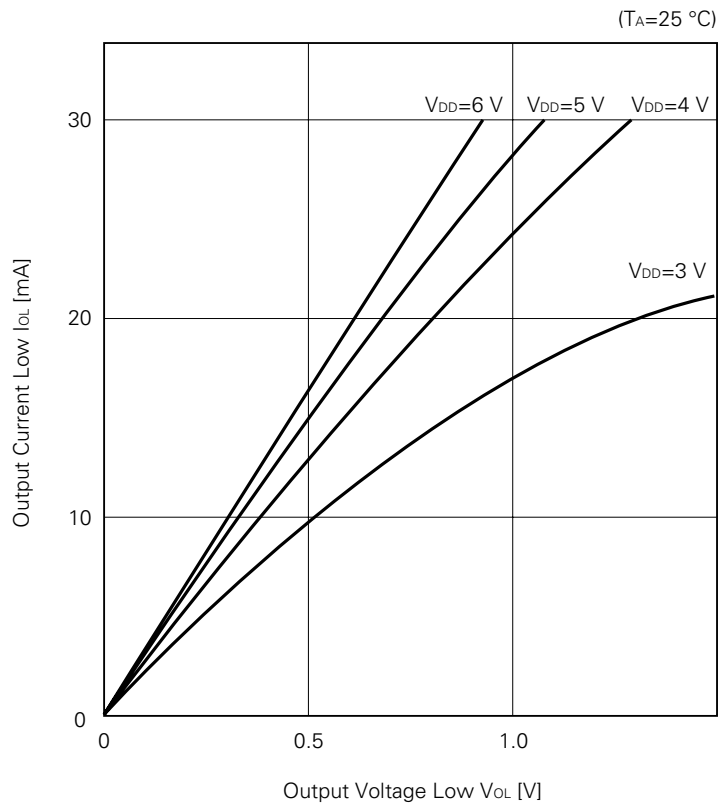
$I_{DD}$  vs  $V_{DD}$  (Main System Clock : 4.19 MHz)



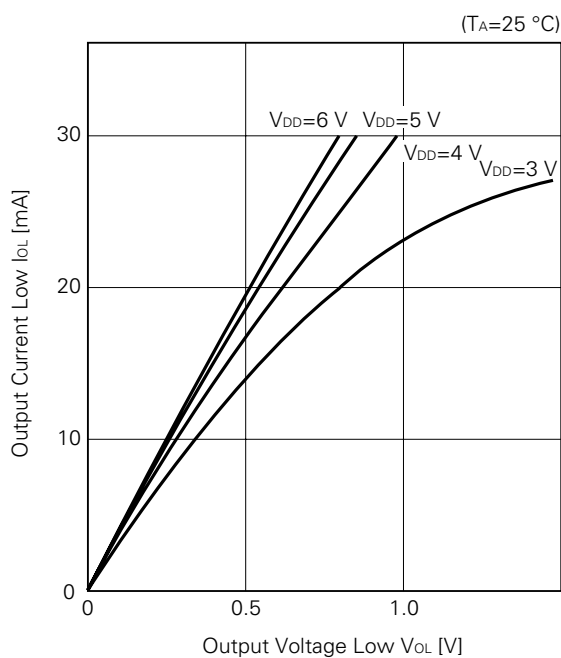
**V<sub>OL</sub> vs I<sub>OL</sub> (Port 0, 2 to 5, P64 to P67)**



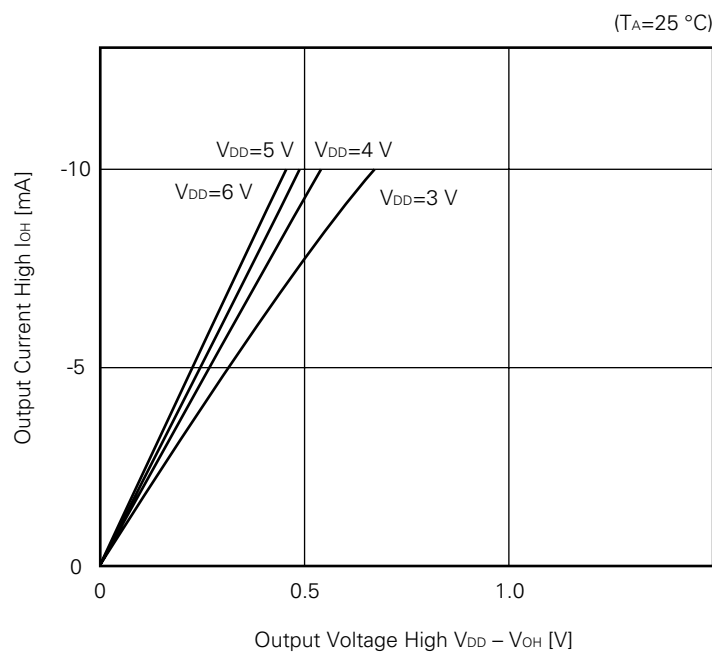
**V<sub>OL</sub> vs I<sub>OL</sub> (P60 to P63)**



**V<sub>OL</sub> vs I<sub>OL</sub> (Port 1)**



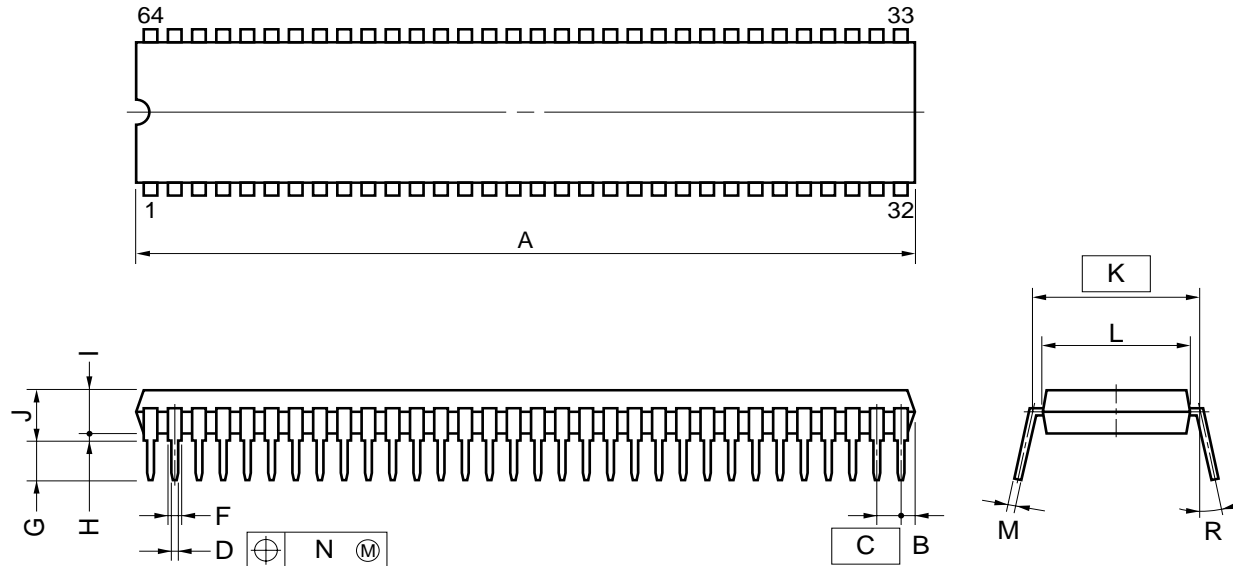
**V<sub>OH</sub> vs I<sub>OH</sub> (Port 0 to 5, P64 to P67)**



# 13. PACKAGE DRAWINGS

## DRAWINGS OF MASS-PRODUCTION PRODUCT PACKAGES (1/2)

### 64-PIN PLASTIC SHRINK DIP (750 mil)



#### NOTE

- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

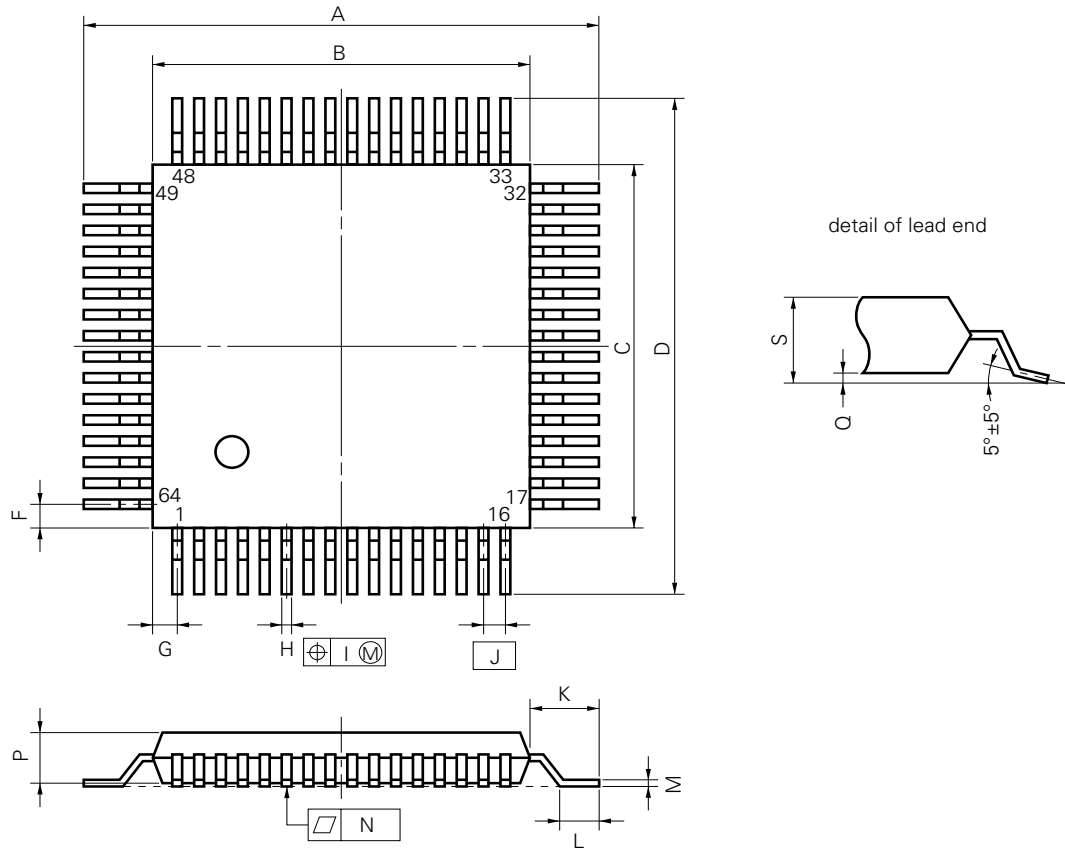
ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	0.020 <sup>+0.004</sup> <sub>-0.005</sub>
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	0.25 <sup>+0.10</sup> <sub>-0.05</sub>	0.010 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

**Caution** Dimensions and materials of ES products are different from those of mass-production products. Refer to DRAWINGS OF ES PRODUCT PACKAGES (1/2).

# DRAWINGS OF MASS-PRODUCTION PRODUCT PACKAGES (2/2)

## 64-PIN PLASTIC QFP (□14)



### NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

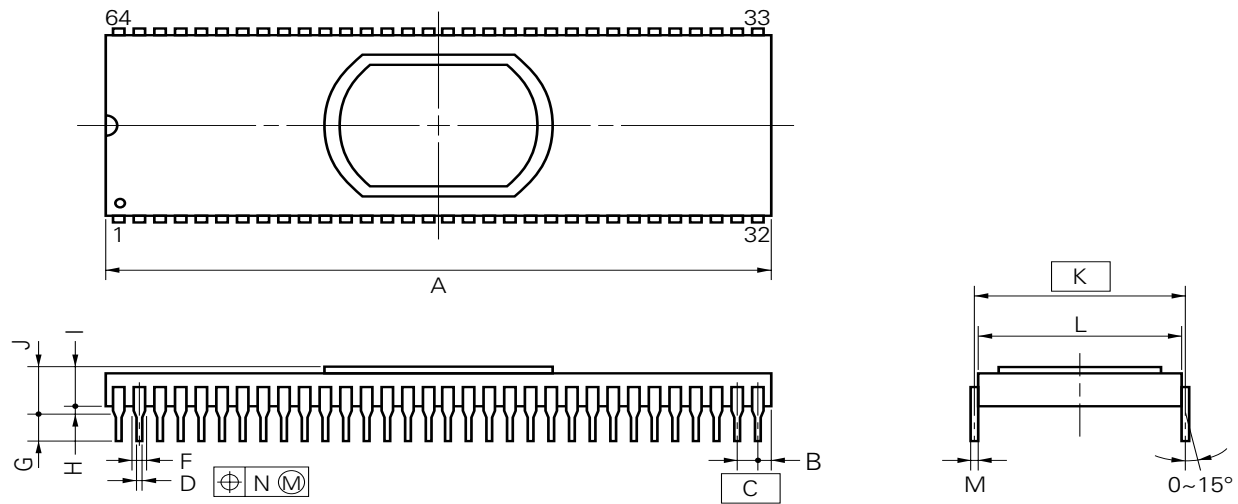
P64GC-80-AB8-3

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
C	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	0.014 <sup>+0.004</sup> <sub>-0.005</sub>
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.15 <sup>+0.10</sup> <sub>-0.05</sub>	0.006 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

**Caution** Dimensions and materials are different from those of mass-production products. Refer to DRAWINGS OF ES PRODUCT PACKAGES (2/2).

# DRAWINGS OF ES PRODUCT PACKAGES (1/2)

## 64PIN CERAMIC SHRINK DIP (SEAM WELD) (750 mil)



### NOTES

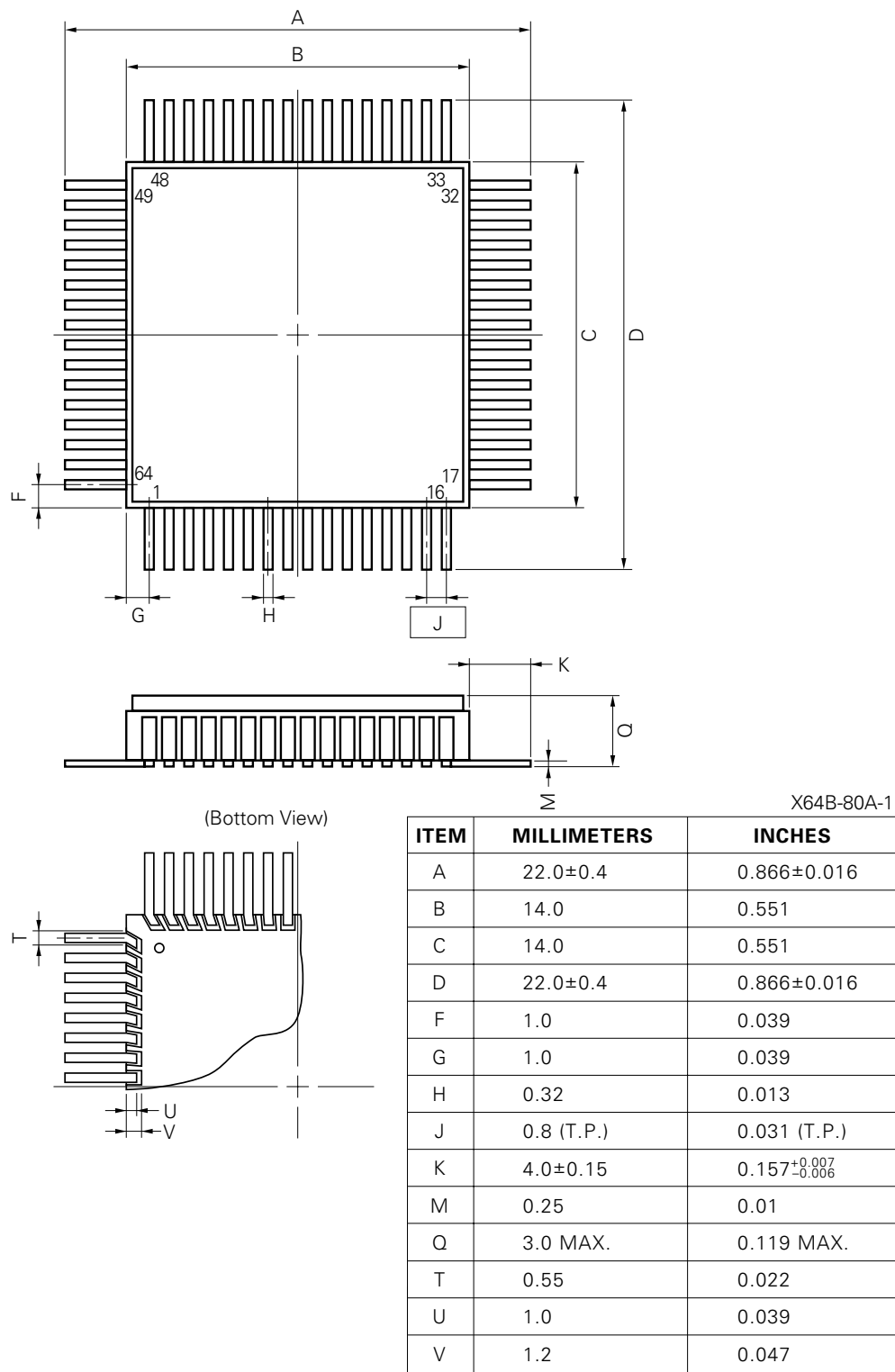
- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

P64D-70-750A1

ITEM	MILLIMETERS	INCHES
A	58.16 MAX.	2.290 MAX.
B	1.521 MAX.	0.060 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.46±0.05	0.018±0.002
F	0.8 MIN.	0.031 MIN.
G	3.5±0.3	0.138±0.012
H	1.02 MIN.	0.040 MIN.
I	3.14	0.124
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	18.8	0.740
M	0.25±0.05	0.010 <sup>+0.002</sup> <sub>-0.003</sub>
N	0.25	0.01

DRAWINGS OF ES PRODUCT PACKAGES (2/2)

64 PIN CERAMIC QFP (14 × 14) (FOR ES)



## 14. RECOMMENDED SOLDERING CONDITIONS

The  $\mu$ PD78001B(A)/78002B(A) should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document “**Semiconductor Device Mounting Technology Manual**” (IEI-1207).

For soldering methods and conditions other than those recommended below, contact our sales personnel.

**Table 14-1 Surface Mounting Type Soldering Conditions**

$\mu$ PD78001BGC(A)-xxx-AB8 : 64-Pin Plastic QFP (□14 mm)

$\mu$ PD78002BGC(A)-xxx-AB8 : 64-Pin Plastic QFP (□14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Twice max. < Points to note > (1) Start the second reflow after the device temperature by the first reflow returns to normal. (2) Flux washing by the water after the first reflow should be avoided.	IR35-00-2
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above) Number of times: Twice max. < Points to note > (1) Start the second reflow after the device temperature by the first reflow returns to normal. (2) Flux washing by the water after the first reflow should be avoided.	VP15-00-2
Pin part heating	Pin temperature: 300°C max., Duration: 3 sec. max. (per device side)	—

**Caution** Use of more than one soldering method should be avoided (except in the case of pin part heating).

**Table 14-2 Insertion Type Soldering Conditions**

$\mu$ PD78001BCW(A)-xxx : 64-Pin Plastic Shrink DIP (750 mil)

$\mu$ PD78002BCW(A)-xxx : 64-Pin Plastic Shrink DIP (750 mil)

Soldering Method	Soldering Conditions
Wave soldering (Pin only)	Solder bath temperature: 260°C max., Duration: 10 sec. max.
Pin part heating	Pin temperature: 300°C max., Duration: 3 sec. max. (per pin)

**Caution** Wave soldering is only for the pins in order that jet solder can not contact with the chip directly.



## APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78001B(A), 78002B(A).

### Language Processing Software

RA78K/0* <sup>1, 2, 3</sup>	78K/0 series common assembler package
CC78K/0* <sup>1, 2, 3</sup>	78K/0 series common C compiler package
DF78002* <sup>1, 2, 3</sup>	μPD78002 subseries device file
CC78K/0-L* <sup>1, 2, 3</sup>	78K/0 series common C compiler library source file

### PROM Programming Tools

PG-1500	PROM programmer
PA-78P014CW PA-78P014GC	Programmer adapter connected to PG-1500
PG-1500 controller* <sup>1, 2</sup>	PG-1500 control program

### Debugging Tools

IE-78000-R	78K/0 series common in-circuit emulator
IE-78000-R-BK	78K/0 series common break board
IE-78014-R-EM	μPD78002/78014 subseries evaluation emulation board
EP-78240CW-R EP-78240GC-R	Emulation probe common to μPD78244 subseries
EV-9200GC-64	Socket to be mounted on user system board created for the 64-pin plastic QFP
SD78K/0* <sup>1, 2</sup>	IE-78000-R screen debugger
SM78K/0* <sup>4, 5, 6</sup>	78K/0 series common system simulator
DF78002* <sup>1, 2, 4, 5</sup>	μPD78002 subseries device file

### Embedded OS

MX78K/0* <sup>1, 2, 3, 6</sup>	78K/0 series common embedded OS
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### Fuzzy Inference Development Support System

FE9000* <sup>1</sup> /FE9200* <sup>5</sup>	Fuzzy knowledge data creation tool
FT9080* <sup>1</sup> /FT9085* <sup>2</sup>	Translator
FI78K0* <sup>1, 2</sup>	Fuzzy inference module
FD78K0* <sup>1, 2</sup>	Fuzzy inference debugger

- \* 1. PC-9800 series (MS-DOS™) based.  
 2. IBM PC/AT™ (PC DOS™) based.  
 3. HP9000 series 300™, HP9000 series 700™ (HP-UX™) based, SPARCstation™, (Sun OS™) based, EWS-4800 series (EWS-UX/V) based.  
 4. PC-9800 series (MS-DOS + Windows™) based.

5. IBM PC/AT (PC DOS + Windows) based.
6. Under development.

**Remarks**

1. For development tools manufactured by a third party, see the "**78K/0 Series Selection Guide**" (IF-1185).
2. RA78K/0, CC78K/0, SD78K/0, and SM78K/0 are used in combination with DF78002.

## APPENDIX B. RELATED DOCUMENTS

### Device Related Documents

Document Name		Document No. (Japanese)	Document No. (English)
User's Manual		IEU-788	IEU-1334
78K/0 Series User's Manual - Instruction		IEU-849	IEU-1372
Application Note	Basic I	IEA-715	IEA-1288
	Basic II	IEA-740	IEA-1299

### Development Tools Documents (User's Manual)

Document Name		Document No. (Japanese)	Document No. (English)
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller		EEU-704	EEU-1291
IE-78000-R		EEU-810	EEU-1398
IE-78000-R-BK		EEU-867	EEU-1427
IE-78014-R-EM		EEU-805	EEU-1400
EP-78240		EEU-986	In preparation
SD78K/0 Screen Debugger	Beginner's guide	EEU-852	EEU-1414
	Reference	EEU-816	EEU-1413

### Embedded Software Documents (User's Manual)

Document Name		Document No. (Japanese)	Document No. (English)
Fuzzy Knowledge Data Creation Tool		EEU-892	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System - Translator		EEU-862	EEU-1444

**Caution** These documents above are subject to change without notice. Be sure to use the latest document for designing your system.

**Other Documents**

Document Name	Document No. (Japanese)	Document No. (English)
Package Manual	IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual	IEI-616	IEI-1207
Quality Grade on NEC Semiconductor Devices	IEI-620	IEI-1209
Semiconductor Device Quality Guarantee Guide	MEI-603	MEI-1202

**Caution** These documents above are subject to change without notice. Be sure to use the latest document for designing your system.

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V<sub>DD</sub> or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

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